

**MODEL NAME :** *DAM00*  
*DAM01*  
**PCB NO :** *LA-F541P*  
**BOM P/N :**

# Dell/Compal Confidential

## Schematic Document

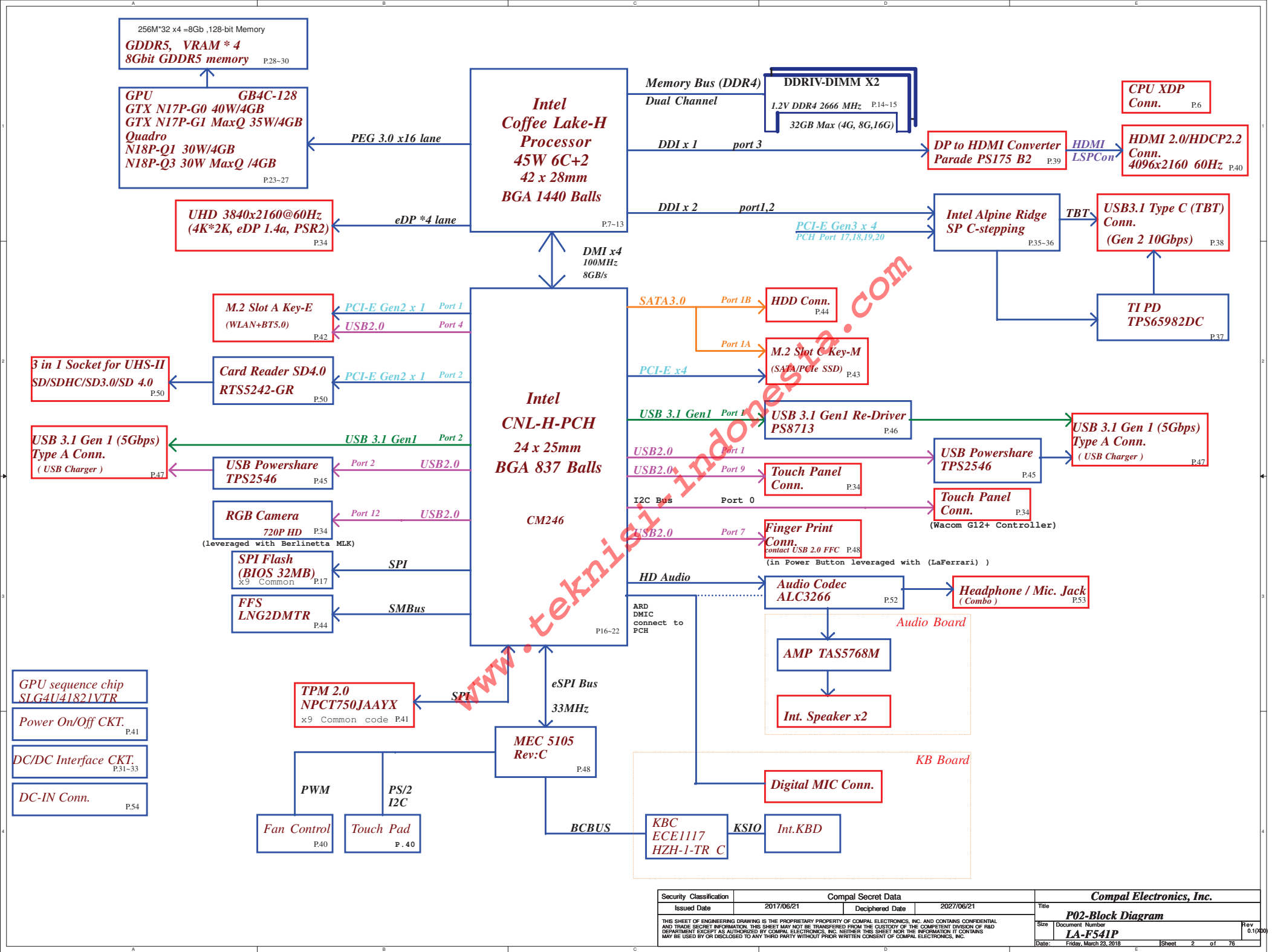
### Berlinetta MLK CFL-H (Coffee Lake-H)

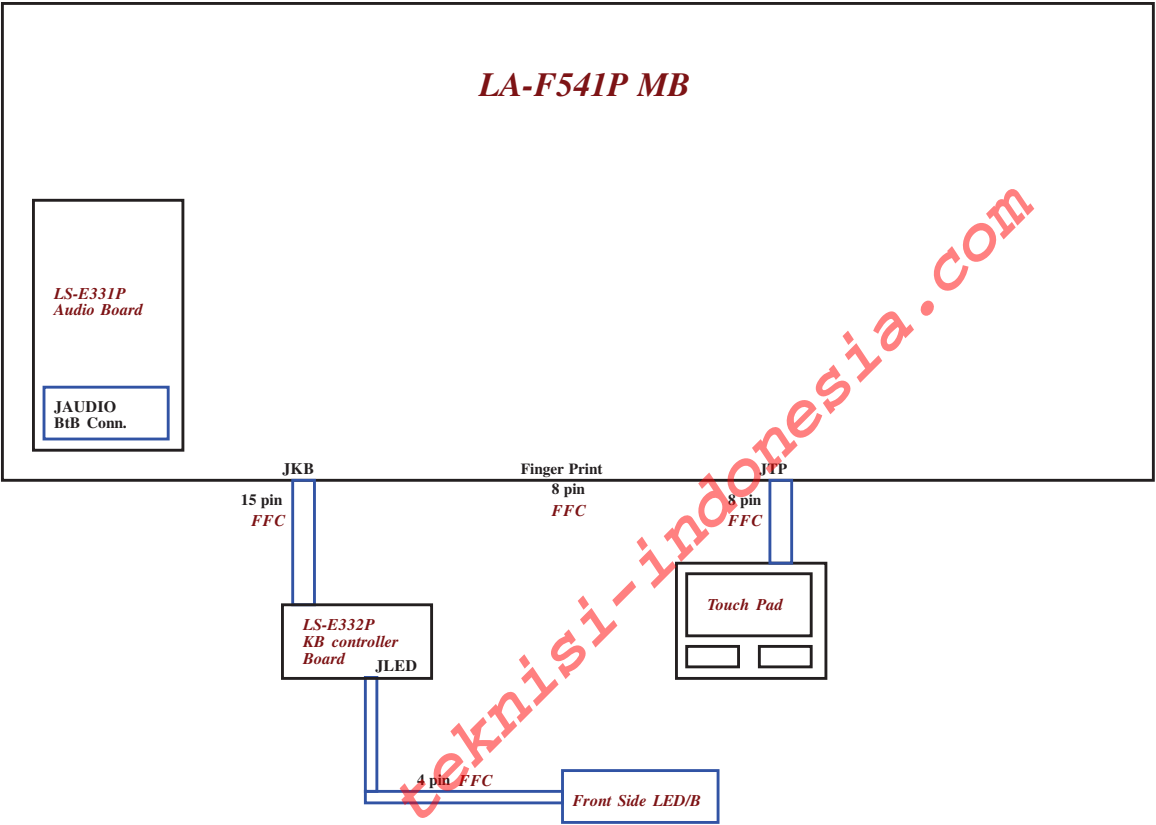
2018-01-10

Rev: DVT2.0

@ : Nopop Component  
NDS3@ : Nopop Component  
XDP@ : Nopop Component  
CONN@ : Connector Component  
R1@ / R3@ : R1/R3 CPN for CPU, GPU, PCB  
TPM@ : TPM function  
EMC@ : Pop of EMI parts  
Q1VRAMS@ : Samsung GDDR5 for Q1-GPU  
Q1VRAMM@ : Micron GDDR5 for Q1-GPU  
G0VRAMS@ : Samsung GDDR5 for G0-GPU  
G0VRAMM@ : Micron GDDR5 for G0-GPU  
G0VRAMH@ : Hynix GDDR5 for G0-GPU  
BreakDown@ : for measure power consumption  
Q1@ : GPU N18PQ1  
G0@ : GPU N17PG0  
UMA@ / DIS@ : UMA/DIS  
CSMB@ :XPS  
BC@ :Perision  
SPAD@ : Nopop Component 0 Ohm Short-PAD for NPI test require  
eSPI@ :eSPI  
G1@ : GPU N17PG1  
Q3@ : GPU N18PQ3

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Issued Date	2017/06/21	Deciphered Date	2027/06/21	Title	
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Board ID	Resistor
X00	240K
X01	130K
X02	
X03	
A00	

USB3.1	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	None
5	None
6	None

USB 2.0	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	NGFF-1 WLAN + BT
5	None
6	None
7	Finger Print
8	None
9	Touch Screen
10	None
11	None
12	RGB CAMERA

USB OC#	DESTINATION
0	USB Conn 1 (Right Side)
1	USB Conn 2 (Left Side)
2	
3	
4	
5	
6	
7	

PCI EXPRESS	DESTINATION	USB3.0	DESTINATION
Lane 1	NGFF-1 WLAN + BT	7	None
Lane 2	None	8	None
Lane 3	None	9	None
Lane 4	None	10	None
Lane 5	CARD READER		
Lane 6	None		
Lane 7	None		
Lane 8	None		
Lane 9	SSD		
Lane 10	SSD	SATA	DESTINATION
Lane 11	SSD	0A	N/A
Lane 12	SSD	1A	SSD
Lane 13	None	0B	N/A
Lane 14	None	1B	N/A
Lane 15	None	2	HDD
Lane 16	None	3	N/A
Lane 17	Alpine Ridge	4	N/A
Lane 18		5	N/A
Lane 19			
Lane 20			

DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	HDMI 2.0

LPC	DESTINATION
ESPI/LPC0	MEC5105
LPC1	DEBUG PORT

CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	None	10	None
1	None	11	None
2	None	12	None
3	NGFF-1 WLAN	13	None
4	CARD READER	14	None
5	Thunderbolt	15	None
6	NGFF-2 SSD		
7	GPU		
8	None		
9	None		

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #2	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7	USB3.1 #8	USB3.1 #9	USB3.1 #10	PCIe #1	PCIe #2	PCIe #3	PCIe #4	PCIe #5	PCIe #6	PCIe #7	PCIe #8	PCIe #9	PCIe #10	PCIe #11	PCIe #12	SATA 0a	SATA 0b	SATA 1a	SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5
Intel® RST Support											No Support	No Support			Yes		No Support		Yes		Yes									

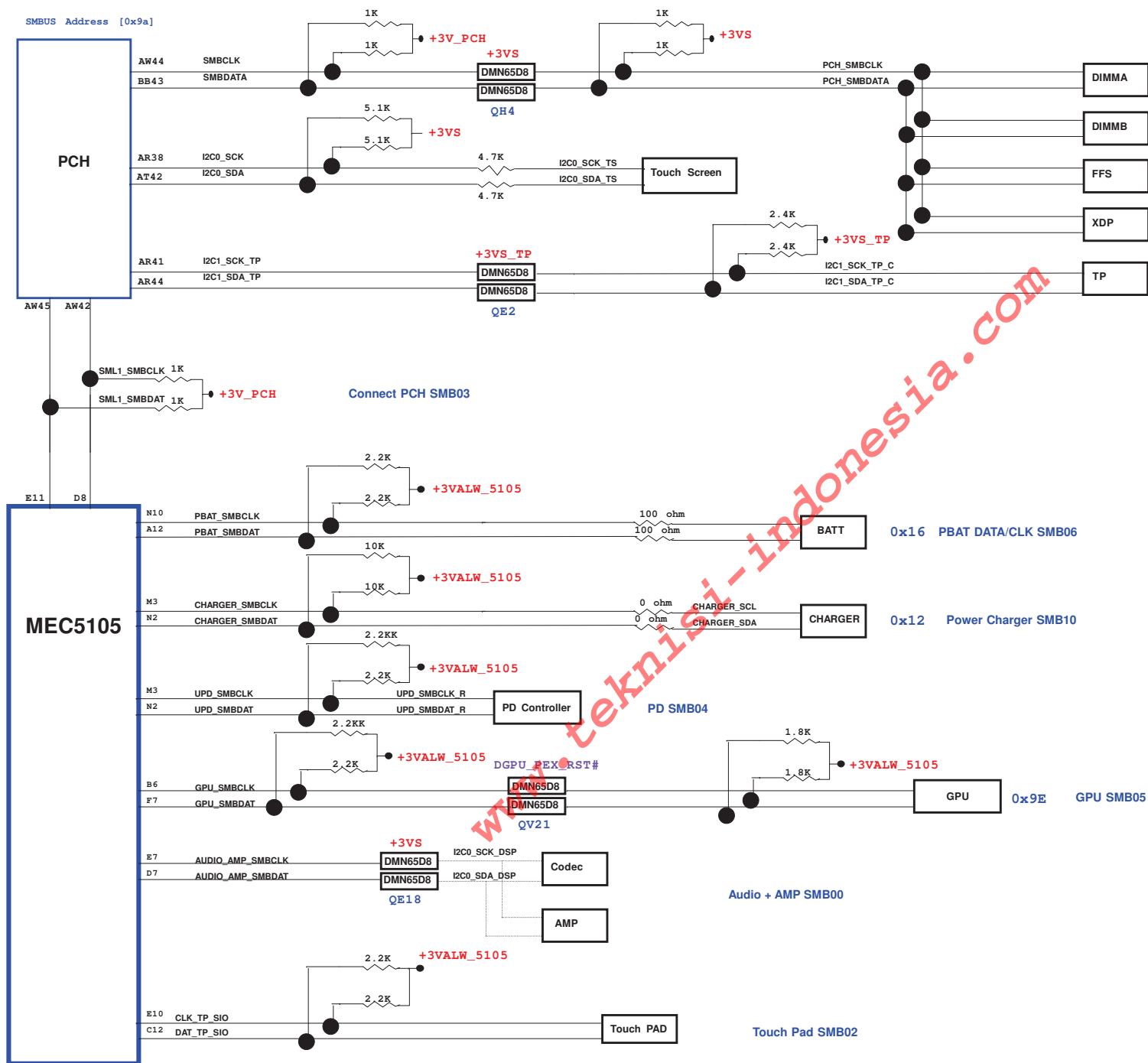
The 30 HSIO lanes on PCB-H supports the following configurations:

- Up to 24 PCIe® Lanes
  - A maximum of 16 PCIe® Ports (or devices) can be enabled
  - When a QoS Port is enabled, the maximum number of PCIe® Ports (or devices) that can be enabled reduces based off the following:
    - Max PCIe® Ports (or devices) = 16 - QoS (0 or 1)
    - PCIe® Lanes 1-4 (PCIe® Controller #1), 5-8 (PCIe® Controller #2), 9-12 (PCIe® Controller #3), 13-16 (PCIe® Controller #4), 17-20 (PCIe® Controller #5), and 21-24 (PCIe® Controller #6) can be individually configured
- Up to 6 SATA Lanes
  - A maximum of 6 SATA Ports (or devices) can be enabled
  - SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
  - SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
- Up to 10 USB 3.1 Lanes
  - A maximum of 10 USB 3.1 Ports (or devices) can be enabled
- Up to 4 QoS Lanes
  - A maximum of 1 QoS Port (or device) can be enabled
- Supports up to 3 Remapped (Intel® Rapid Storage Technology) PCIe® storage devices
  - #2 and #4 PCIe® NVMe SSD
  - #2 Intel® Optane® Memory Device
- See the "PCI Express" (PCIe®) chapter for the PCI PCIe® Controllers, configurations, and Lanes that can be used for Intel® Rapid Storage Technology PCIe® storage support
- For unused SATA/PCIe® Combo Lanes, Flex I/O Lanes that can be configured as PCIe® or SATA, the lanes must be statically assigned to SATA or PCIe® via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the Intel® Flash Image Tool (FIT) tool.

Symbol Note :

 : means Digital Ground  : means Analog Ground

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<23> PEG\_HTX\_C\_GRX\_P0\_15] << PEG\_HTX\_C\_GRX\_P0\_15] << PEG\_HTX\_C\_GRX\_N0\_15] << PEG\_HTX\_C\_GRX\_N0\_15] << PEG\_GTX\_C\_HRX\_P0\_15] << PEG\_GTX\_C\_HRX\_P0\_15] << PEG\_GTX\_C\_HRX\_N0\_15] << PEG\_GTX\_C\_HRX\_N0\_15]

+VCCIO

RH24

1 2 24.9 0201 1%

PEG\_ROMP

Trace Width/Space: 15 mil/ 15 mil  
Max Trace Length: 400 mil

<18> DMI\_CRX\_PTX\_P0 << DMI\_CRX\_PTX\_N0 <18> DMI\_CRX\_PTX\_P1 << DMI\_CRX\_PTX\_N1 <18> DMI\_CRX\_PTX\_P2 << DMI\_CRX\_PTX\_N2 <18> DMI\_CRX\_PTX\_P3 << DMI\_CRX\_PTX\_N3

D8 DMI\_RXP\_0 DMI\_RXN\_0 E8 DMI\_RXP\_1 DMI\_RXN\_1 F8 DMI\_RXP\_2 DMI\_RXN\_2 J8 DMI\_RXP\_3 DMI\_RXN\_3

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CFI-H\_BGA1440

@

To Alpine Ridge

To Alpine Ridge

To DP to HDMI Converter (UMI/P5175B2)

CFI-H

UHD

K36 DDH1\_TXP\_0 EDP\_TXP\_0 K37 DDH1\_TXN\_0 EDP\_TXN\_0 J36 DDH1\_TXP\_1 EDP\_TXP\_1 J37 DDH1\_TXN\_1 EDP\_TXN\_1 H37 DDH1\_TXP\_2 EDP\_TXP\_2 H38 DDH1\_TXN\_2 EDP\_TXN\_2 J37 DDH1\_TXP\_3 EDP\_TXP\_3 J38 DDH1\_TXN\_3 EDP\_TXN\_3

D27 DDH1\_AUXP EDP\_AUXP D28 DDH1\_AUXN EDP\_AUXN

H34 DDH2\_TXP\_0 EDP\_TXP\_0 H35 DDH2\_TXN\_0 EDP\_TXN\_0 F37 DDH2\_TXP\_1 EDP\_TXP\_1 F38 DDH2\_TXN\_1 EDP\_TXN\_1 F34 DDH2\_TXP\_2 EDP\_TXP\_2 F35 DDH2\_TXN\_2 EDP\_TXN\_2 E37 DDH2\_TXP\_3 EDP\_TXP\_3 E38 DDH2\_TXN\_3 EDP\_TXN\_3

F26 DDH2\_AUXP EDP\_AUXP F27 DDH2\_AUXN EDP\_AUXN

G34 DDH3\_TXP\_0 EDP\_TXP\_0 G35 DDH3\_TXN\_0 EDP\_TXN\_0 B34 DDH3\_TXP\_1 EDP\_TXP\_1 B35 DDH3\_TXN\_1 EDP\_TXN\_1 E33 DDH3\_TXP\_2 EDP\_TXP\_2 E34 DDH3\_TXN\_2 EDP\_TXN\_2 C33 DDH3\_TXP\_3 EDP\_TXP\_3 C34 DDH3\_TXN\_3 EDP\_TXN\_3

A27 DDH3\_AUXP EDP\_AUXP A28 DDH3\_AUXN EDP\_AUXN

CFI-H\_BGA1440

@

CFI-H

UHD

E25 PEG\_GTX\_C\_HRX\_P15 EDP\_TXP\_0 D25 PEG\_GTX\_C\_HRX\_N15 EDP\_TXN\_0

F24 PEG\_GTX\_C\_HRX\_P14 EDP\_TXP\_1 D24 PEG\_GTX\_C\_HRX\_N14 EDP\_TXN\_1

E23 PEG\_GTX\_C\_HRX\_P13 EDP\_TXP\_2 D23 PEG\_GTX\_C\_HRX\_N13 EDP\_TXN\_2

F22 PEG\_GTX\_C\_HRX\_P12 EDP\_TXP\_3 D22 PEG\_GTX\_C\_HRX\_N12 EDP\_TXN\_3

E21 PEG\_GTX\_C\_HRX\_P11 EDP\_TXP\_4 D21 PEG\_GTX\_C\_HRX\_N11 EDP\_TXN\_4

F20 PEG\_GTX\_C\_HRX\_P10 EDP\_TXP\_5 D20 PEG\_GTX\_C\_HRX\_N10 EDP\_TXN\_5

E19 PEG\_GTX\_C\_HRX\_P9 EDP\_TXP\_6 D19 PEG\_GTX\_C\_HRX\_N9 EDP\_TXN\_6

F18 PEG\_GTX\_C\_HRX\_P8 EDP\_TXP\_7 D18 PEG\_GTX\_C\_HRX\_N8 EDP\_TXN\_7

E17 PEG\_GTX\_C\_HRX\_P7 EDP\_TXP\_8 D17 PEG\_GTX\_C\_HRX\_N7 EDP\_TXN\_8

F16 PEG\_GTX\_C\_HRX\_P6 EDP\_TXP\_9 D16 PEG\_GTX\_C\_HRX\_N6 EDP\_TXN\_9

E15 PEG\_GTX\_C\_HRX\_P5 EDP\_TXP\_10 D15 PEG\_GTX\_C\_HRX\_N5 EDP\_TXN\_10

F14 PEG\_GTX\_C\_HRX\_P4 EDP\_TXP\_11 D14 PEG\_GTX\_C\_HRX\_N4 EDP\_TXN\_11

E13 PEG\_GTX\_C\_HRX\_P3 EDP\_TXP\_12 D13 PEG\_GTX\_C\_HRX\_N3 EDP\_TXN\_12

F12 PEG\_GTX\_C\_HRX\_P2 EDP\_TXP\_13 D12 PEG\_GTX\_C\_HRX\_N2 EDP\_TXN\_13

E11 PEG\_GTX\_C\_HRX\_P1 EDP\_TXP\_14 D11 PEG\_GTX\_C\_HRX\_N1 EDP\_TXN\_14

F10 PEG\_GTX\_C\_HRX\_P0 EDP\_TXP\_15 D10 PEG\_GTX\_C\_HRX\_N0 EDP\_TXN\_15

E10 PEG\_GTX\_C\_HRX\_P0 EDP\_TXP\_15 D10 PEG\_GTX\_C\_HRX\_N0 EDP\_TXN\_15

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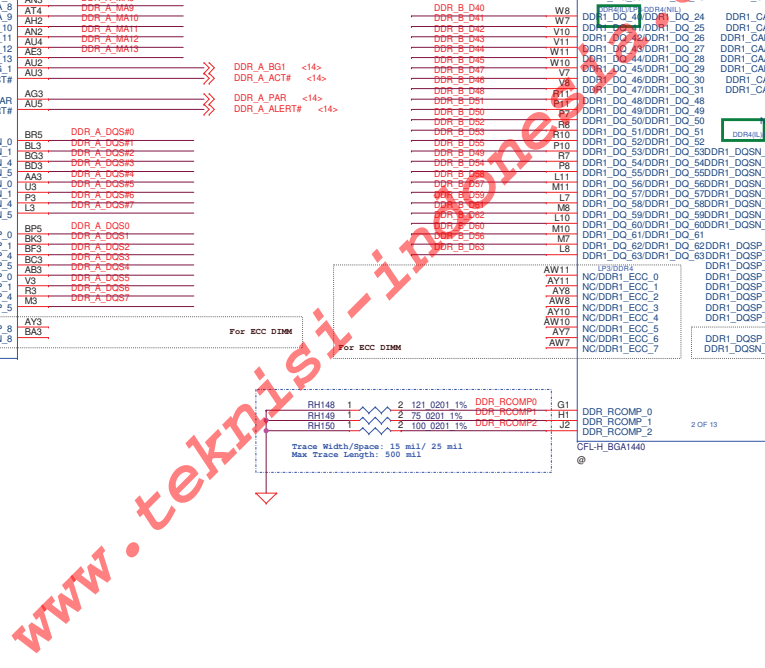
E10 PEG\_GTX\_C\_HRX\_P0 EDP\_TXP\_15 D10 PEG\_GTX\_C\_HRX\_N0 EDP\_TXN\_15

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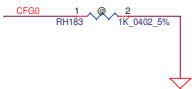


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## CFG Straps for Processor

Stall reset sequence after PCU PLL lock until de-asserted

CFG0	<p>* 1 = (Default) Normal Operation; No stall.</p> <p>0 = Stall.</p>
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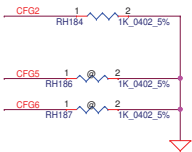
## Display Port Presence Strap

CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port
	* 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



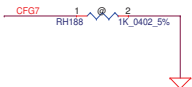
## PCIE Port Bifurcation Straps

```
CFG[6:5]  *11: (Default) x16 - Device 1 functions 1 and 2 disabled
          10: x8, x8 - Device 1 function 1 enabled ; function 2
             disabled
          01: Reserved - (Device 1 function 1 disabled ; function
             2 enabled)
          00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```



## PEG DEFER TRAINING

```
CFG7      * 1: (Default) PEG Train immediately following xx
           de assertion
           0: PEG Wait for BIOS for training
```



**Table 2-13. PCI Express\* Bifurcation and Lane Reversal Mapping**

Configuration	Link Width			CFG Signals			Lanes															
	0:10	0:11	0:12	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10 <td>11</td> <td>12</td> <td>13</td> <td>14</td> <td>15</td>	11	12	13	14	15
x16 reversed	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8 reversed	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x8+2x4 reversed	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

For CFG bus details, refer to [Section 6.4](#).  
 Support is also provided for narrow width and further devices with lower number of lanes (that is, usage on x4 configuration).  
 However reverse lanes are not supported.  
 In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:

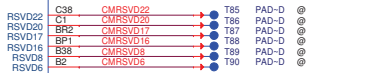
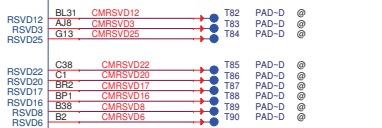
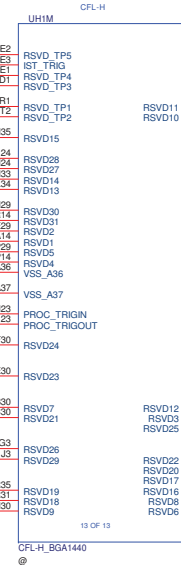
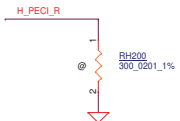
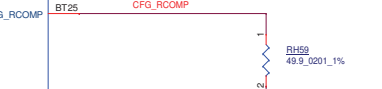
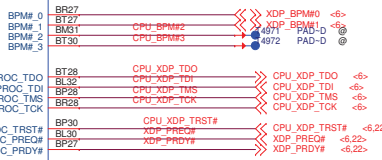
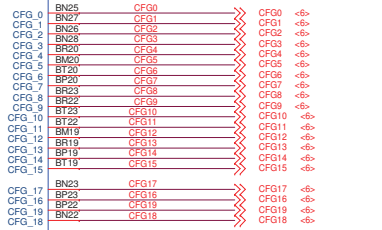
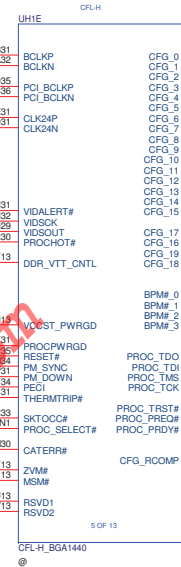
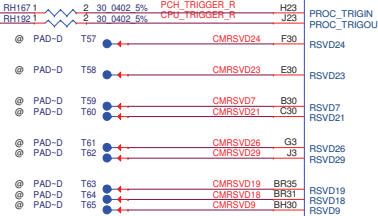
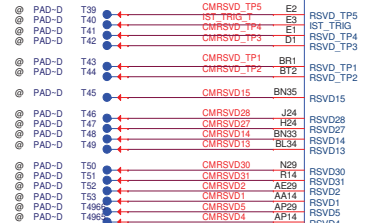
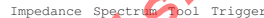
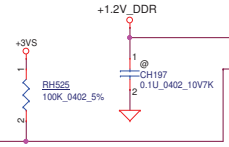
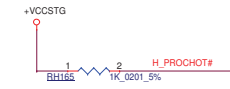
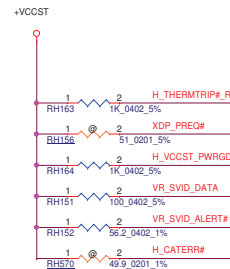
- Connect lane 0 of 1<sup>st</sup> device to lane 0.
- Connect lane 0 of 2<sup>nd</sup> device to lane 8.
- Connect lane 0 of 3<sup>rd</sup> device to lane 12.

For example:

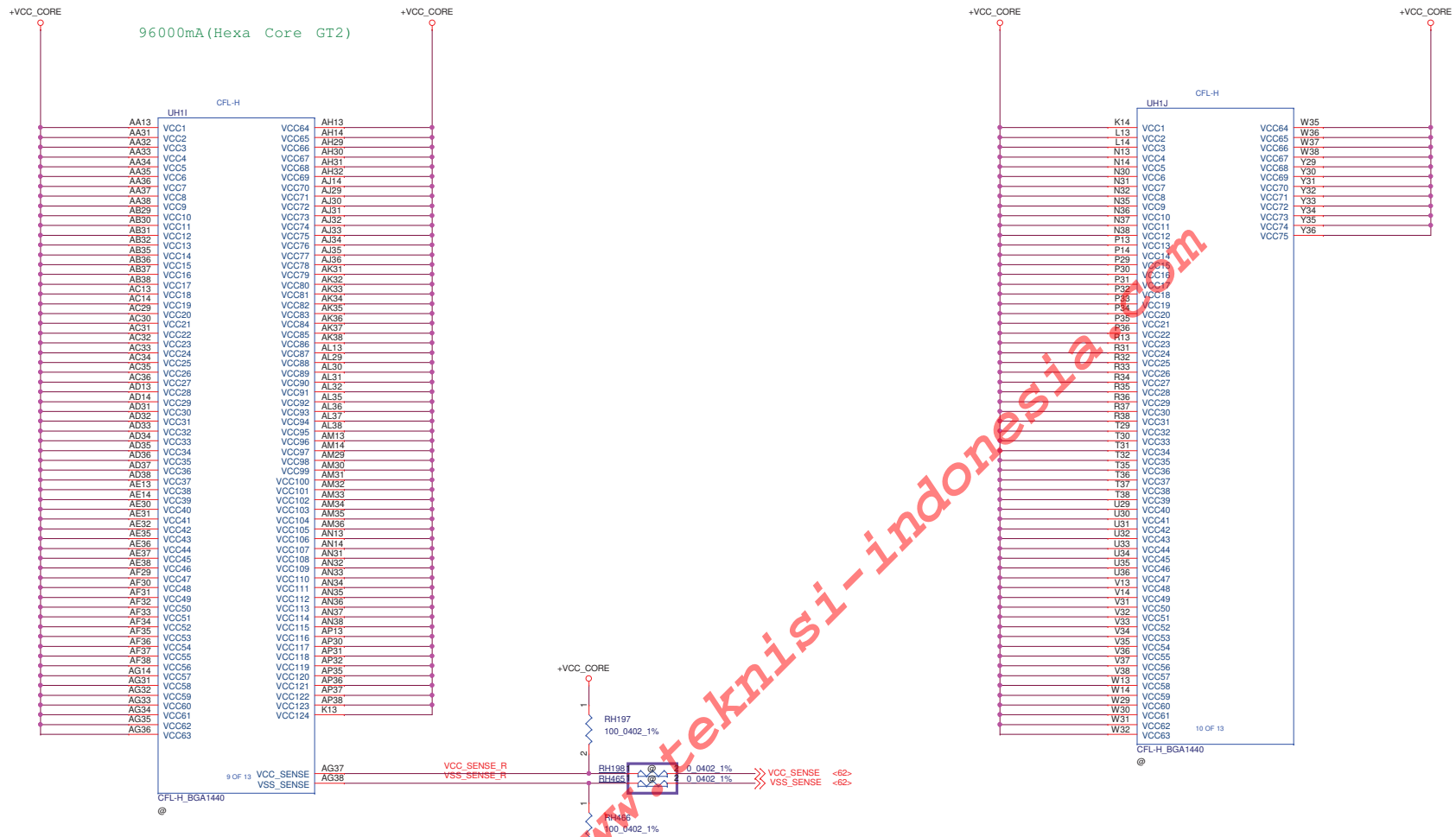
- a. When using 1x8 + 2x4, the 4 lane device should use lanes 0:7.
- b. When using 1x4 + 1x2, the 4 lane device should use lanes 0:3 and other 2 lanes device should use lanes 8:9.
- c. When using 1x4 + 1x2 + 1x1, 4 lane device should use lanes 0:3, two 2 lane device should use lanes 8:9, one 1 lane device should use lane 16.

For reverse lanes, for example:

- When using 1x8, the 8 lane device should use lanes 8:15, so lane 15 will be connected to lane 0 of the Device.
- For Basin Falls platform use 1x2 + 1x4 Bifurcation

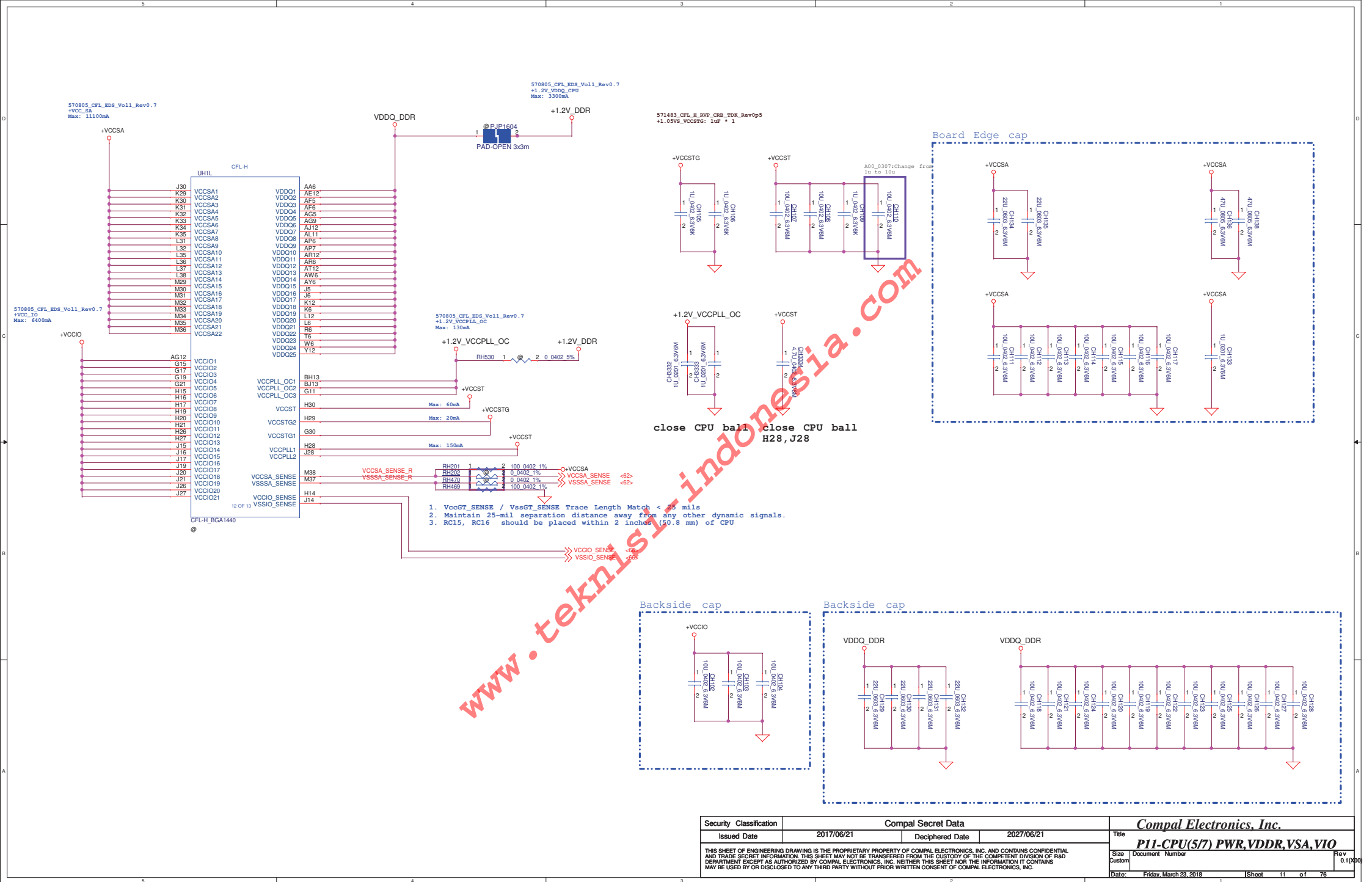


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				Sheet	
				9	
				o/f	76

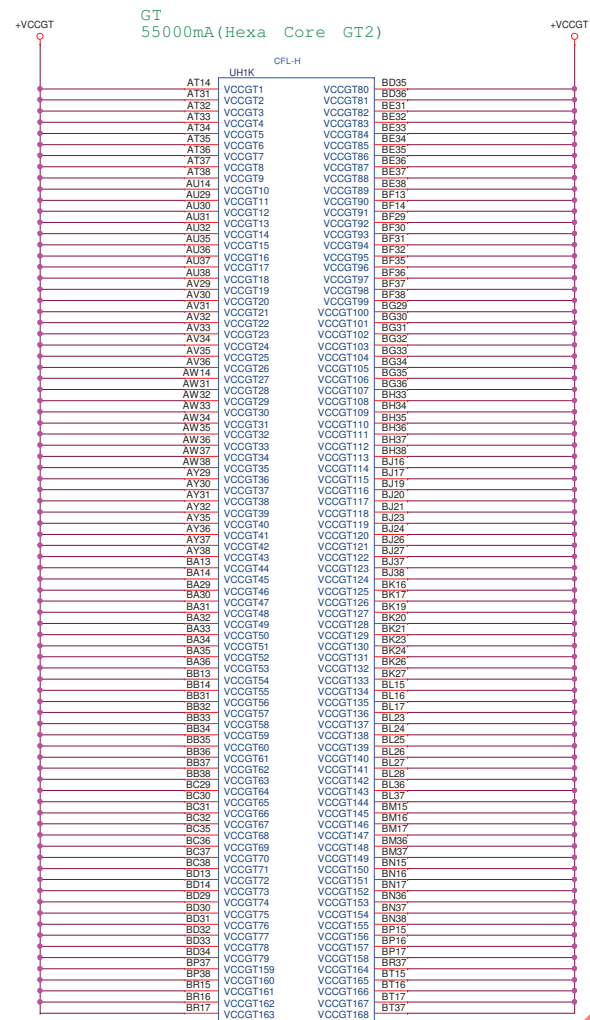


1. Vcc\_SENSE/ Vss\_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC10, RC11 should be placed within 2 inches (50.8 mm) of CPU

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								Size	Document Number	Rev
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1. VccGT\_SENSE / VssGT\_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC12, RC13 should be placed within 2 inches (50.8 mm) of CPU

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CFL-H		
UH1F		
A10	VSS_1	VSS_82
A12	VSS_2	VSS_83
A16	VSS_3	VSS_84
A18	VSS_4	VSS_85
A20	VSS_5	VSS_86
A22	VSS_6	VSS_87
A24	VSS_7	VSS_88
A26	VSS_8	VSS_89
A28	VSS_9	VSS_90
A30	VSS_10	VSS_91
A6	VSS_11	VSS_92
A9	VSS_12	VSS_93
AA12	VSS_13	VSS_94
AA29	VSS_14	VSS_95
AA30	VSS_15	VSS_96
AB33	VSS_16	VSS_97
AB34	VSS_17	VSS_98
AB6	VSS_18	VSS_99
AC1	VSS_19	VSS_100
AC12	VSS_20	VSS_101
AC2	VSS_21	VSS_102
AC3	VSS_22	VSS_103
AC37	VSS_23	VSS_104
AC38	VSS_24	VSS_105
AC4	VSS_25	VSS_106
AC5	VSS_26	VSS_107
AC6	VSS_27	VSS_108
AD10	VSS_28	VSS_109
AD11	VSS_29	VSS_110
AD12	VSS_30	VSS_111
AD29	VSS_31	VSS_112
AD30	VSS_32	VSS_113
AD6	VSS_33	VSS_114
AD8	VSS_34	VSS_115
AD9	VSS_35	VSS_116
AE33	VSS_36	VSS_117
AE6	VSS_37	VSS_118
AF1	VSS_38	VSS_119
AF12	VSS_39	VSS_120
AF13	VSS_40	VSS_121
AF14	VSS_41	VSS_122
AF2	VSS_42	VSS_123
AF3	VSS_43	VSS_124
AF4	VSS_44	VSS_125
AG10	VSS_45	VSS_126
AG11	VSS_46	VSS_127
AG13	VSS_47	VSS_128
AG29	VSS_48	VSS_129
AG30	VSS_49	VSS_130
AG6	VSS_50	VSS_131
AG7	VSS_51	VSS_132
AG8	VSS_52	VSS_133
AH12	VSS_53	VSS_134
AH33	VSS_54	VSS_135
AH34	VSS_55	VSS_136
AH35	VSS_56	VSS_137
AH36	VSS_57	VSS_138
AH6	VSS_58	VSS_139
AJ1	VSS_59	VSS_140
AJ13	VSS_60	VSS_141
AJ2	VSS_61	VSS_142
AJ3	VSS_62	VSS_143
AJ37	VSS_63	VSS_144
AJ38	VSS_64	VSS_145
AJ4	VSS_65	VSS_146
AJ5	VSS_66	VSS_147
AJ6	VSS_67	VSS_148
W4	VSS_68	VSS_149
W5	VSS_69	VSS_150
V12	VSS_70	VSS_151
Y10	VSS_71	VSS_152
Y11	VSS_72	VSS_153
Y13	VSS_73	VSS_154
Y14	VSS_74	VSS_155
Y37	VSS_75	VSS_156
Y38	VSS_76	VSS_157
Y7	VSS_77	VSS_158
Y8	VSS_78	VSS_159
Y9	VSS_79	VSS_160
AK29	VSS_80	VSS_161
AK30	VSS_81	VSS_162

CFL-H, BGA1440  
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CFL-H		
UH1G		
AW5	VSS_163	VSS_244
AY12	VSS_164	VSS_245
AY33	VSS_165	VSS_246
AY34	VSS_166	VSS_247
B8	VSS_167	VSS_248
BA10	VSS_168	VSS_249
BA11	VSS_169	VSS_250
BA12	VSS_170	VSS_251
BA37	VSS_171	VSS_252
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BB3	VSS_180	VSS_261
BB30	VSS_181	VSS_262
BB5	VSS_182	VSS_263
BB4	VSS_183	VSS_264
BB5	VSS_184	VSS_265
BC12	VSS_185	VSS_266
BC13	VSS_186	VSS_267
BC14	VSS_187	VSS_268
BC33	VSS_188	VSS_269
BC34	VSS_189	VSS_270
BC6	VSS_190	VSS_271
BD10	VSS_191	VSS_272
BD11	VSS_192	VSS_273
BD12	VSS_193	VSS_274
BD37	VSS_194	VSS_275
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BE4	VSS_204	VSS_285
BE5	VSS_205	VSS_286
BE6	VSS_206	VSS_287
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BF34	VSS_209	VSS_290
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BG12	VSS_211	VSS_292
BG13	VSS_212	VSS_293
BG14	VSS_213	VSS_294
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BH8	VSS_228	VSS_309
BH9	VSS_229	VSS_310
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I3	VSS_231	VSS_312
I33	VSS_232	VSS_313
I34	VSS_233	VSS_314
I4	VSS_234	VSS_315
I5	VSS_235	VSS_316
I7	VSS_236	VSS_317
I8	VSS_237	VSS_318
I9	VSS_238	VSS_319
I37	VSS_239	VSS_320
I38	VSS_240	VSS_321
I39	VSS_241	VSS_322
I42	VSS_242	VSS_323
I44	VSS_243	VSS_324

CFL-H, BGA1440  
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CFL-H		
UH1H		
BN4	VSS_325	VSS_409
BN7	VSS_326	VSS_410
BP12	VSS_327	VSS_411
BP14	VSS_328	VSS_412
BP16	VSS_329	VSS_413
BP21	VSS_330	VSS_414
BP24	VSS_331	VSS_415
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BP7	VSS_337	VSS_421
BR12	VSS_338	VSS_422
BR14	VSS_339	VSS_423
BR18	VSS_340	VSS_424
BR21	VSS_341	VSS_425
BR24	VSS_342	VSS_426
BR25	VSS_343	VSS_427
BR26	VSS_344	VSS_428
BR29	VSS_345	VSS_429
BR4	VSS_346	VSS_430
BR7	VSS_347	VSS_431
BT12	VSS_348	VSS_432
BT14	VSS_349	VSS_433
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BT24	VSS_352	VSS_436
BT26	VSS_353	VSS_437
BT29	VSS_354	VSS_438
BT32	VSS_355	VSS_439
BT5	VSS_356	VSS_440
C11	VSS_357	VSS_441
C13	VSS_358	VSS_442
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C23	VSS_363	VSS_447
C25	VSS_364	VSS_448
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C27	VSS_366	VSS_450
C31	VSS_367	VSS_451
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D18	VSS_376	VSS_460
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D22	VSS_378	VSS_462
D24	VSS_379	VSS_463
D26	VSS_380	VSS_464
D28	VSS_381	VSS_465
D3	VSS_382	VSS_466
D30	VSS_383	VSS_467
D33	VSS_384	VSS_468
D6	VSS_385	VSS_469
D9	VSS_386	VSS_470
E34	VSS_387	VSS_471
E35	VSS_388	VSS_472
E38	VSS_389	VSS_473
E4	VSS_390	VSS_474
E9	VSS_391	VSS_475
N3	VSS_392	VSS_476
N33	VSS_393	VSS_477
N34	VSS_394	VSS_478
N4	VSS_395	VSS_479
N5	VSS_396	
N6	VSS_397	VSS_A3
N7	VSS_398	VSS_A34
N8	VSS_399	VSS_A4
N9	VSS_400	VSS_B3
P12	VSS_401	VSS_B37
P37	VSS_402	VSS_BR38
M14	VSS_403	VSS_BT3
M6	VSS_404	VSS_BT35
N1	VSS_405	VSS_BT36
F11	VSS_406	VSS_BT4
F13	VSS_407	VSS_C2
F13	VSS_408	VSS_D38

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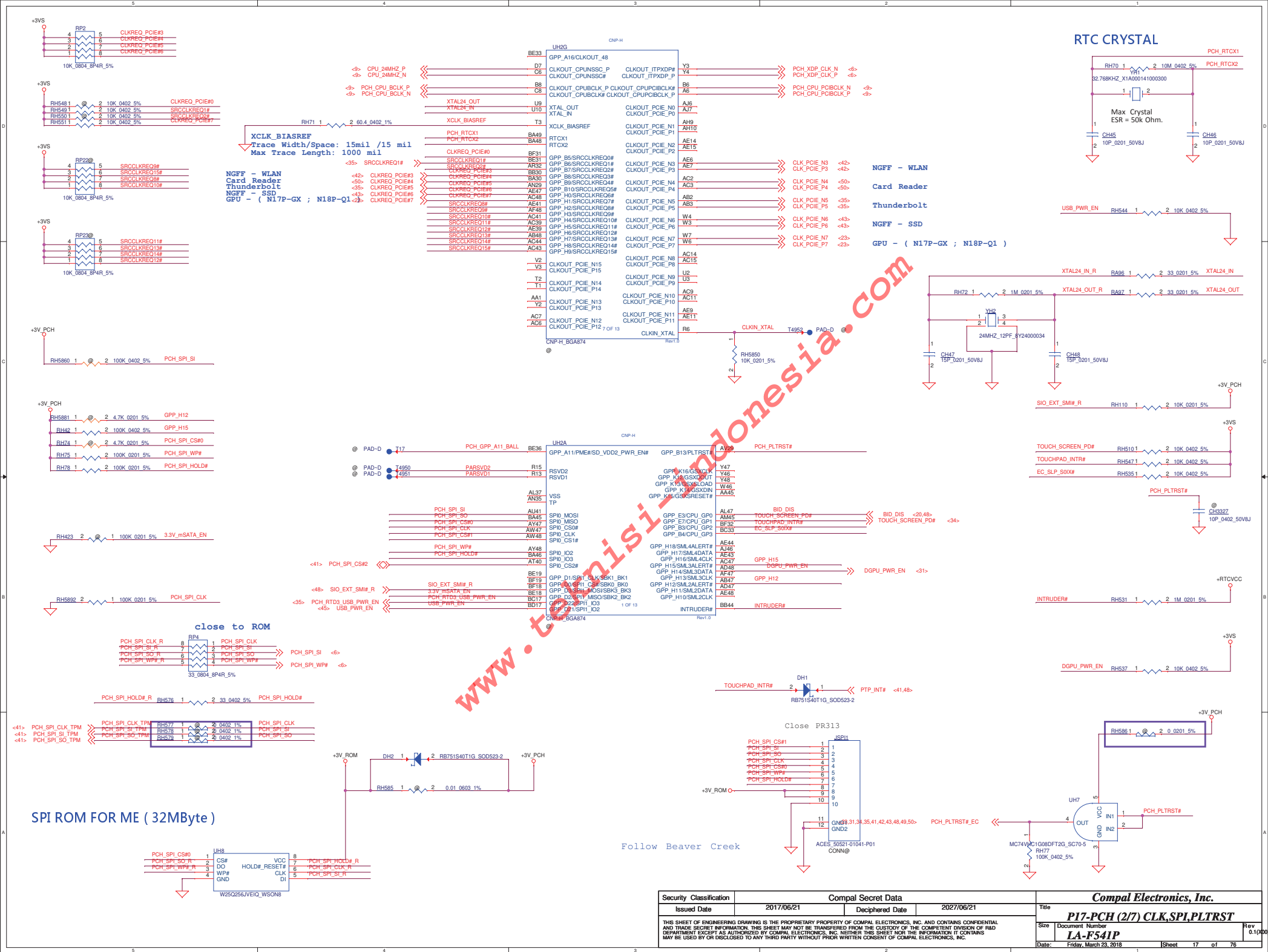
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P13-CPU(7/7) VSS

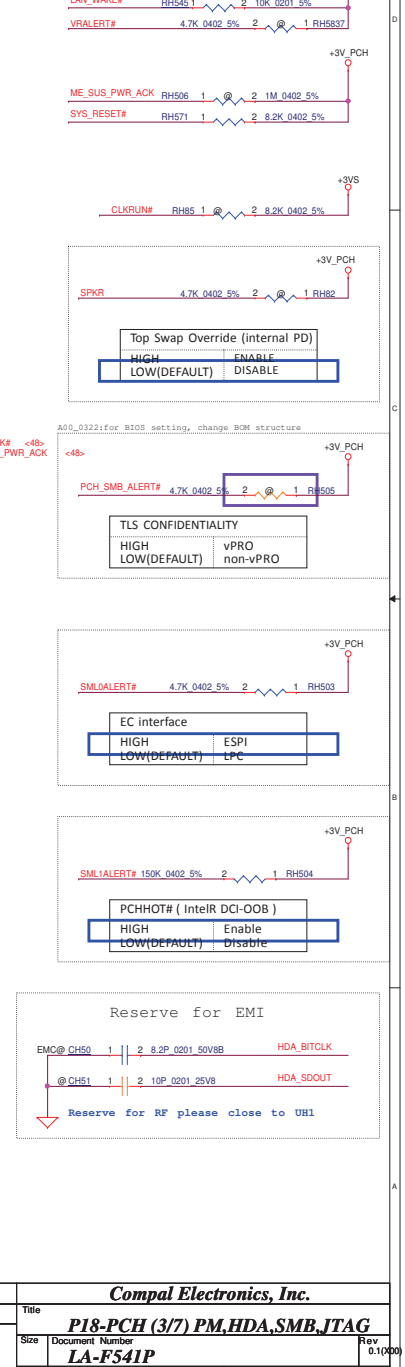
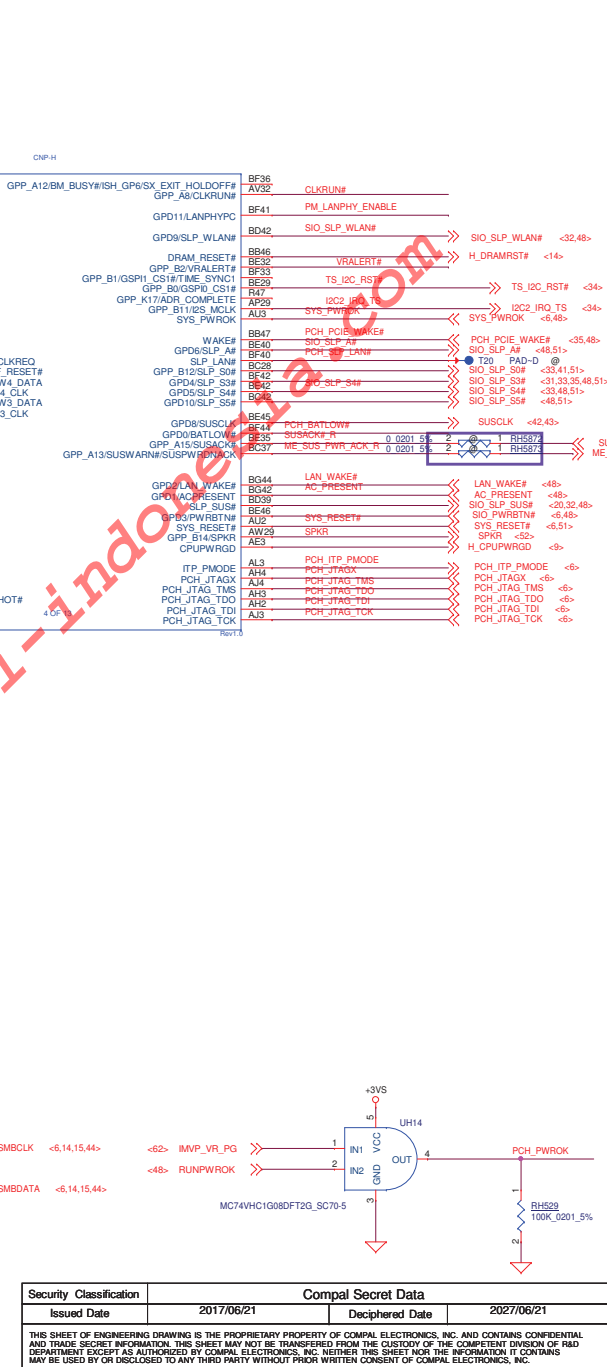
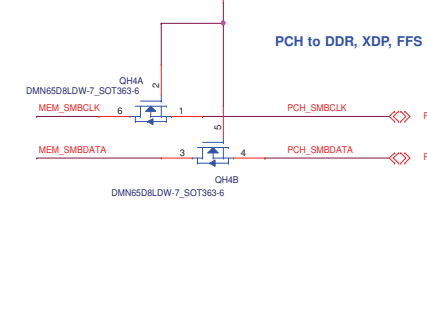
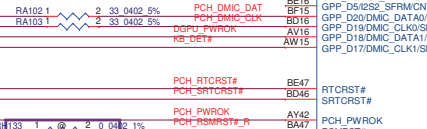
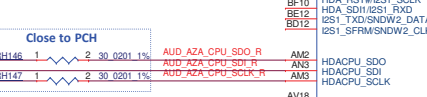
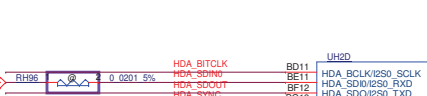
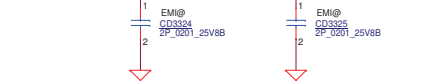
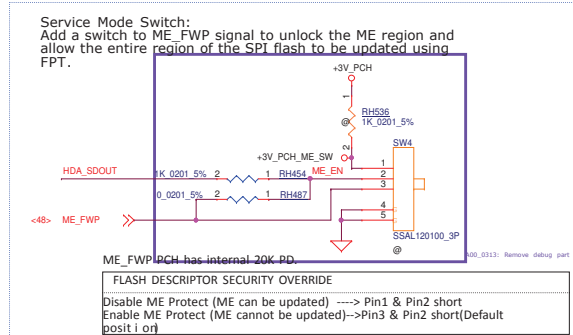
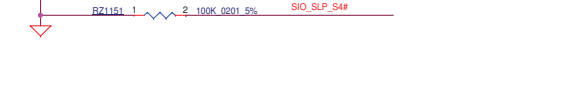
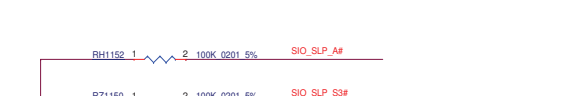
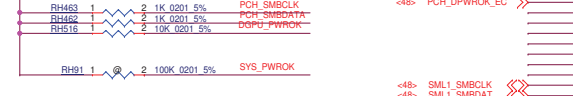
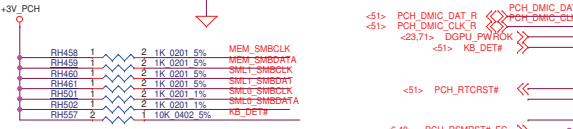
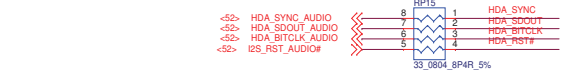


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HDA\_SDO / I2S0\_TXD  
ME\_FWP PCH has internal 20K PD.  
FLASH DESCRIPTOR SECURITY OVERRIDE  
1=Disable ME Protect (ME can be updated)  
0=Enable ME Protect (ME cannot be updated)



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7- DMI CTX\_PRX\_N0  
7- DMI CTX\_PRX\_P0  
7- DMI CTX\_PTX\_N0  
7- DMI CTX\_PTX\_P0  
7- DMI CTX\_PTX\_N1  
7- DMI CTX\_PTX\_P1  
7- DMI CTX\_PTX\_N2  
7- DMI CTX\_PTX\_P2  
7- DMI CTX\_PTX\_N3  
7- DMI CTX\_PTX\_P3

NGFF  
42- PCIE\_PRX\_DTX\_N1  
42- PCIE\_PRX\_DTX\_P1  
42- PCIE\_PRX\_DTX\_N2  
42- PCIE\_PRX\_DTX\_P2

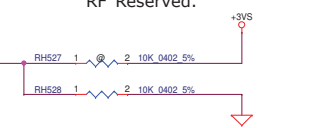
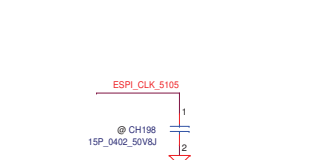
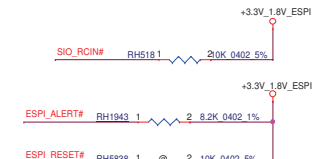
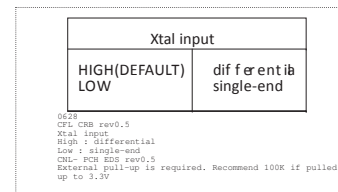
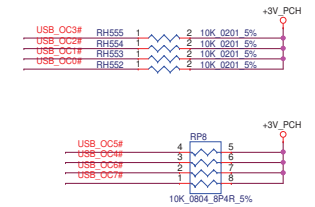
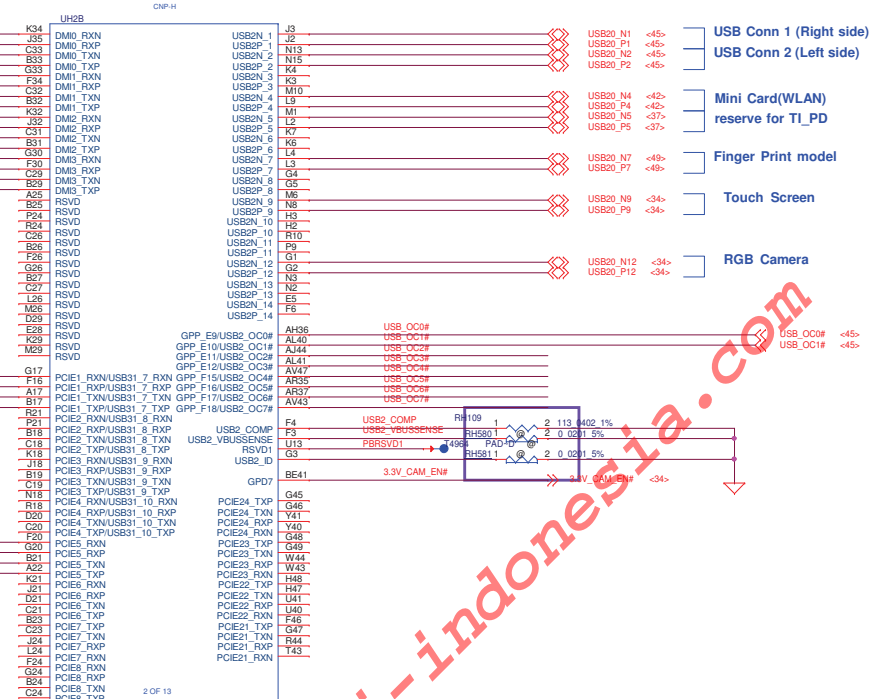
CARD\_READER  
50- PCIE\_PRX\_DTX\_N5  
50- PCIE\_PRX\_DTX\_P5  
50- PCIE\_PRX\_DTX\_N6  
50- PCIE\_PRX\_DTX\_P6

USB Conn JUSB2 (Bottom Right Side)

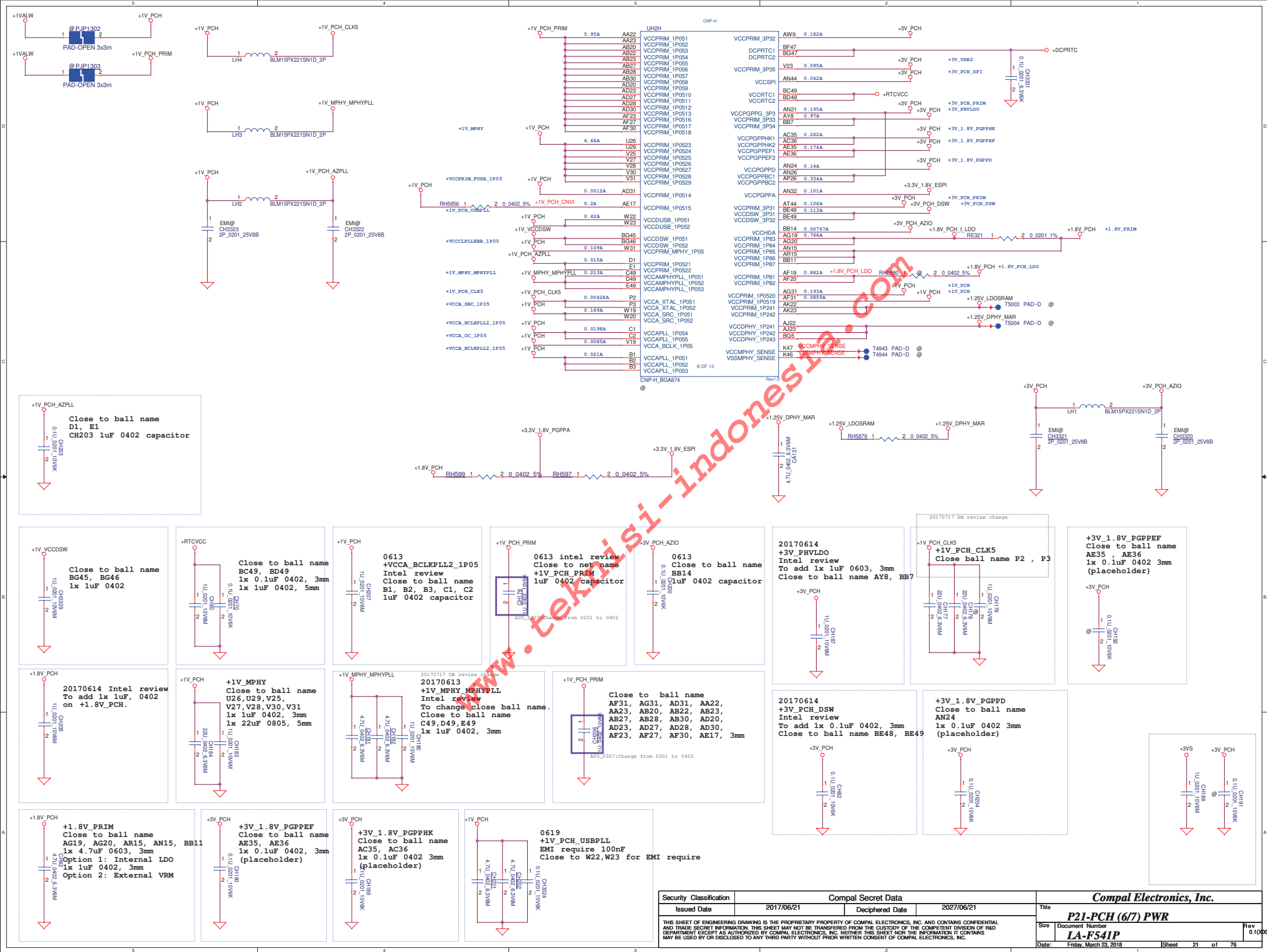
USB Conn JUSB1 (Bottom Left Side)

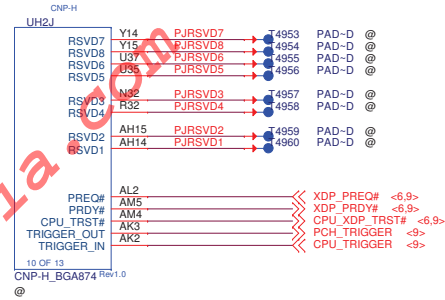
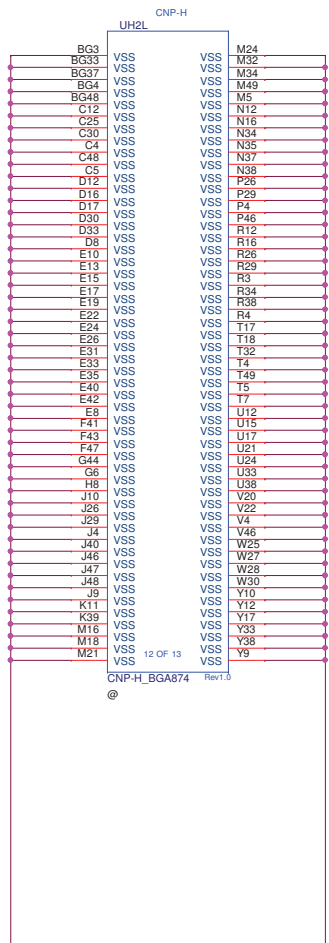
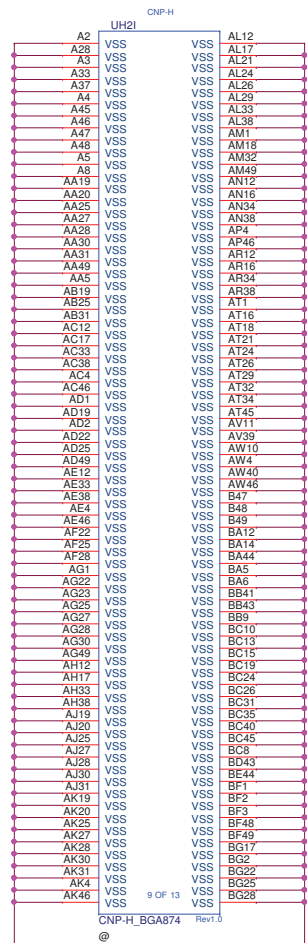
46- USB3\_PTX\_DRX\_N1  
46- USB3\_PTX\_DRX\_P1  
46- USB3\_PTX\_DRX\_N2  
46- USB3\_PTX\_DRX\_P2  
47- USB3\_PTX\_DRX\_N3  
47- USB3\_PTX\_DRX\_P3  
47- USB3\_PTX\_DRX\_N4  
47- USB3\_PTX\_DRX\_P4

47- USB3\_PTX\_DRX\_N1  
47- USB3\_PTX\_DRX\_P1  
47- USB3\_PTX\_DRX\_N2  
47- USB3\_PTX\_DRX\_P2  
47- USB3\_PTX\_DRX\_N3  
47- USB3\_PTX\_DRX\_P3  
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47- USB3\_PTX\_DRX\_P4

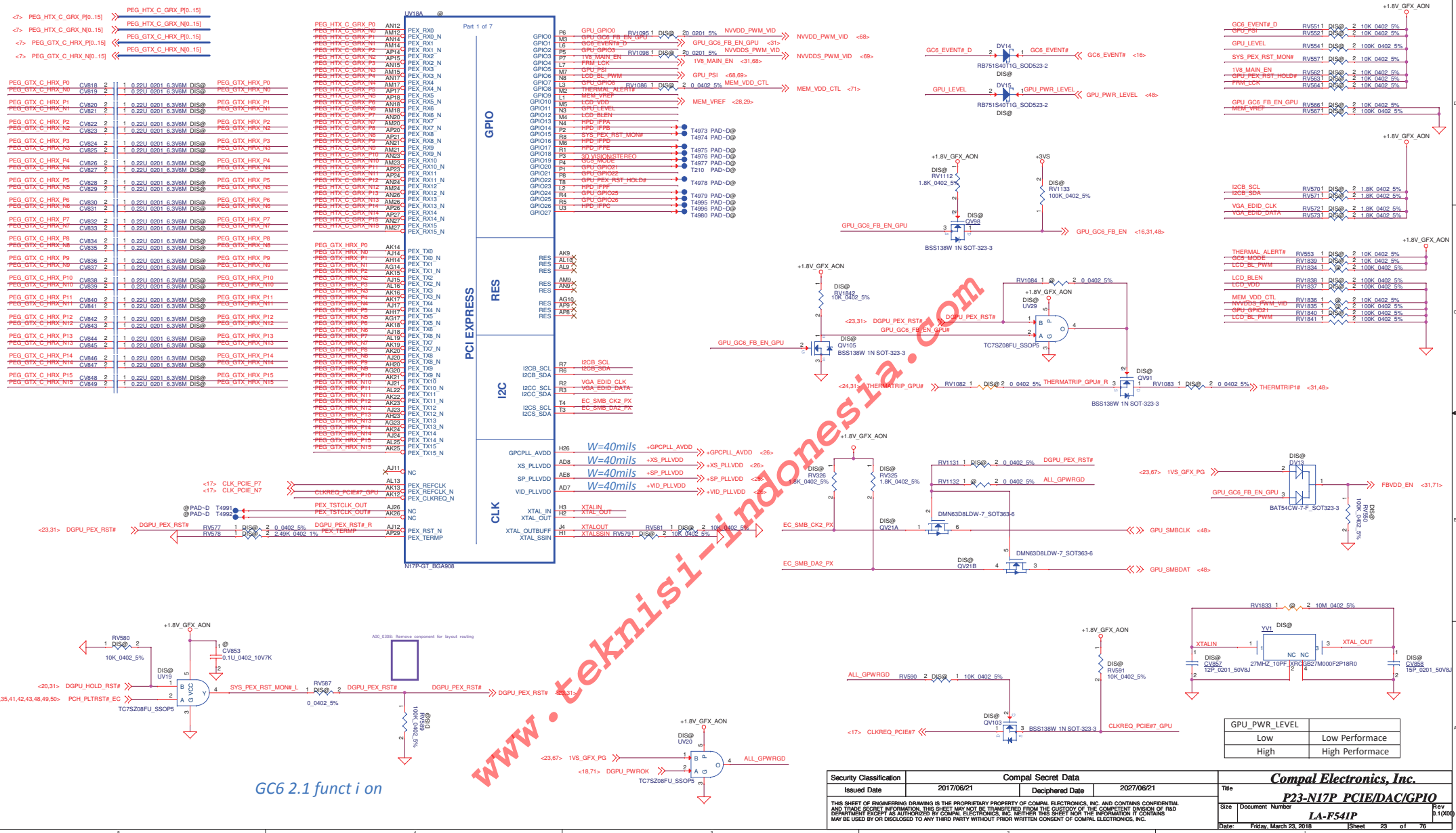


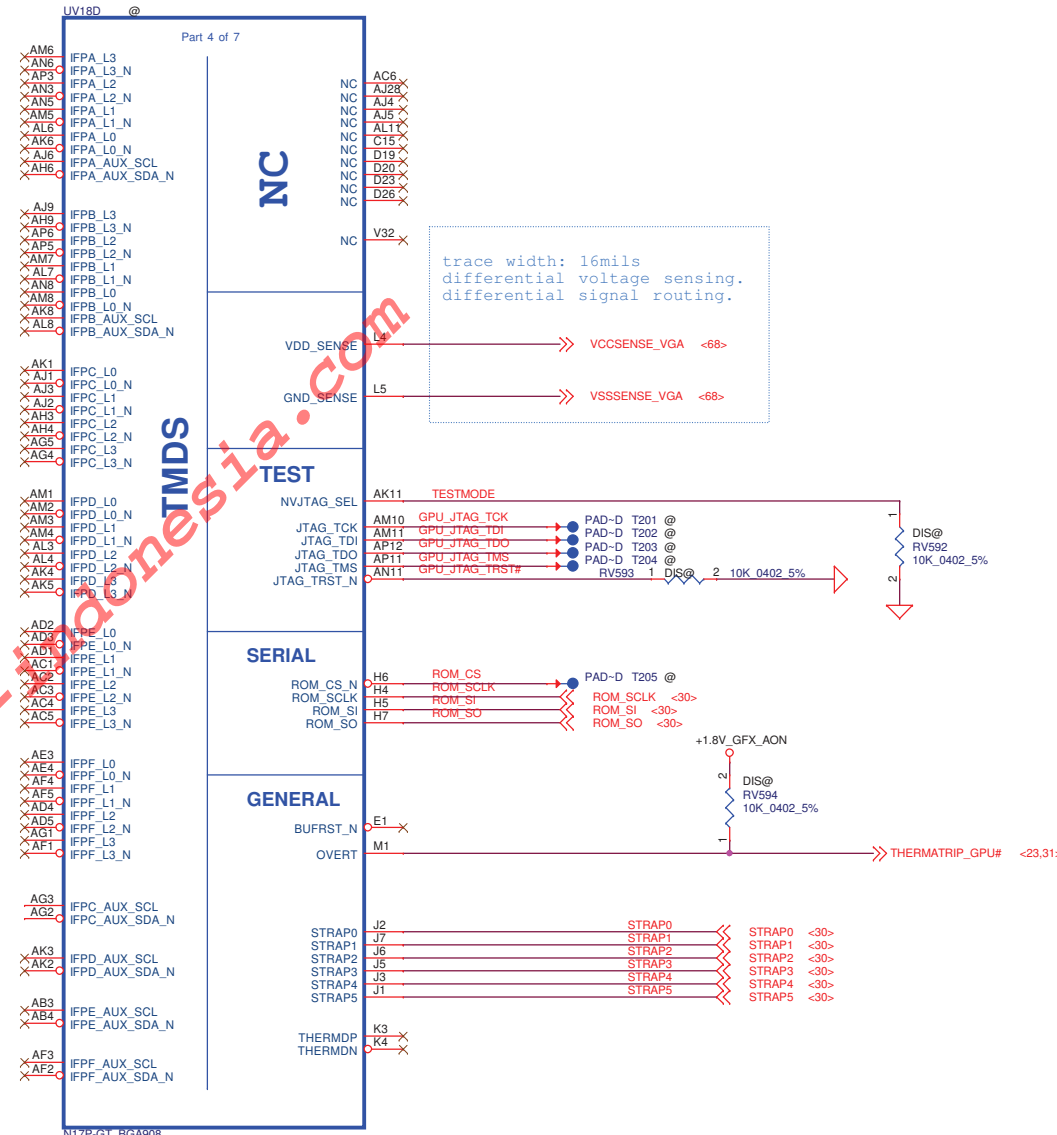


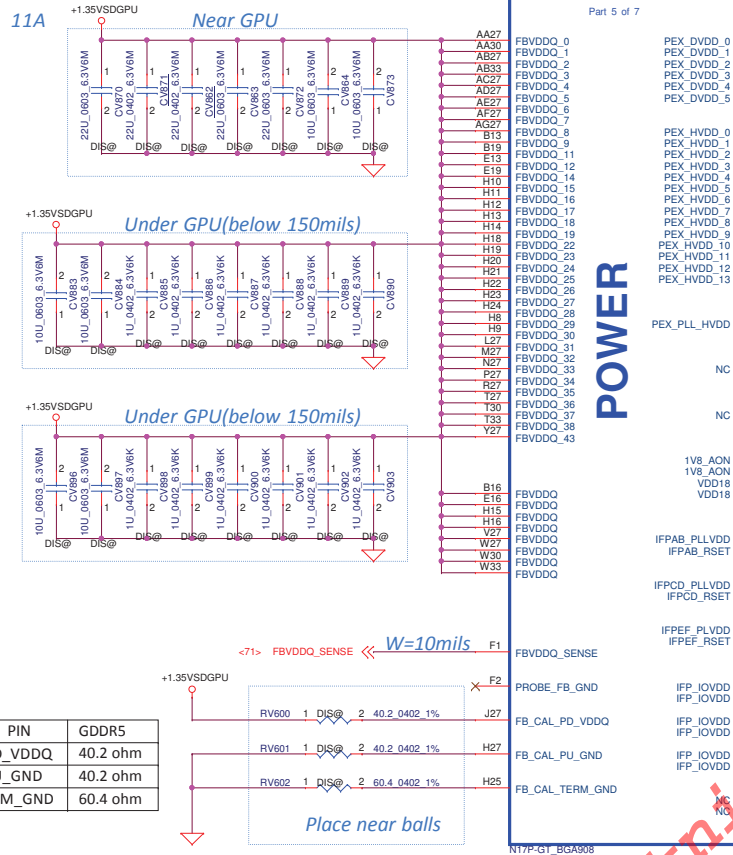




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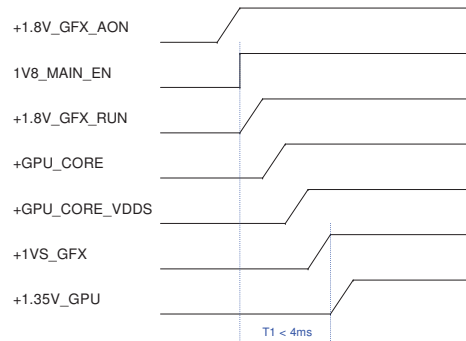






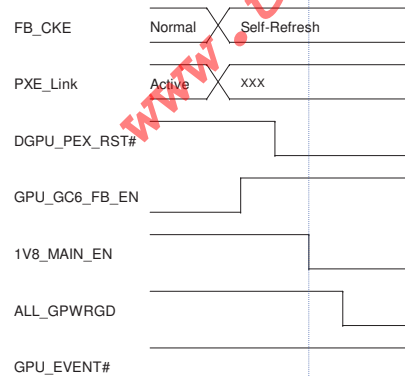
CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2 ohm
FB_CAL_x_PU_GND	40.2 ohm
FB_CAL_xTERM_GND	60.4 ohm

## GPU Power Up Sequence



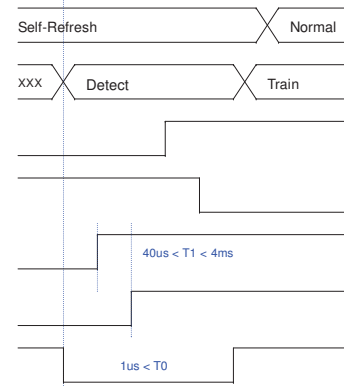
The ramp time for any rail must be more than 40us and less than 2ms.

## GPU GC6 Entry Sequence

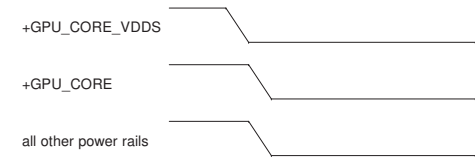


The entire entry/exit sequence must complete within 200 ms.

## GPU GC6 Exit Sequence

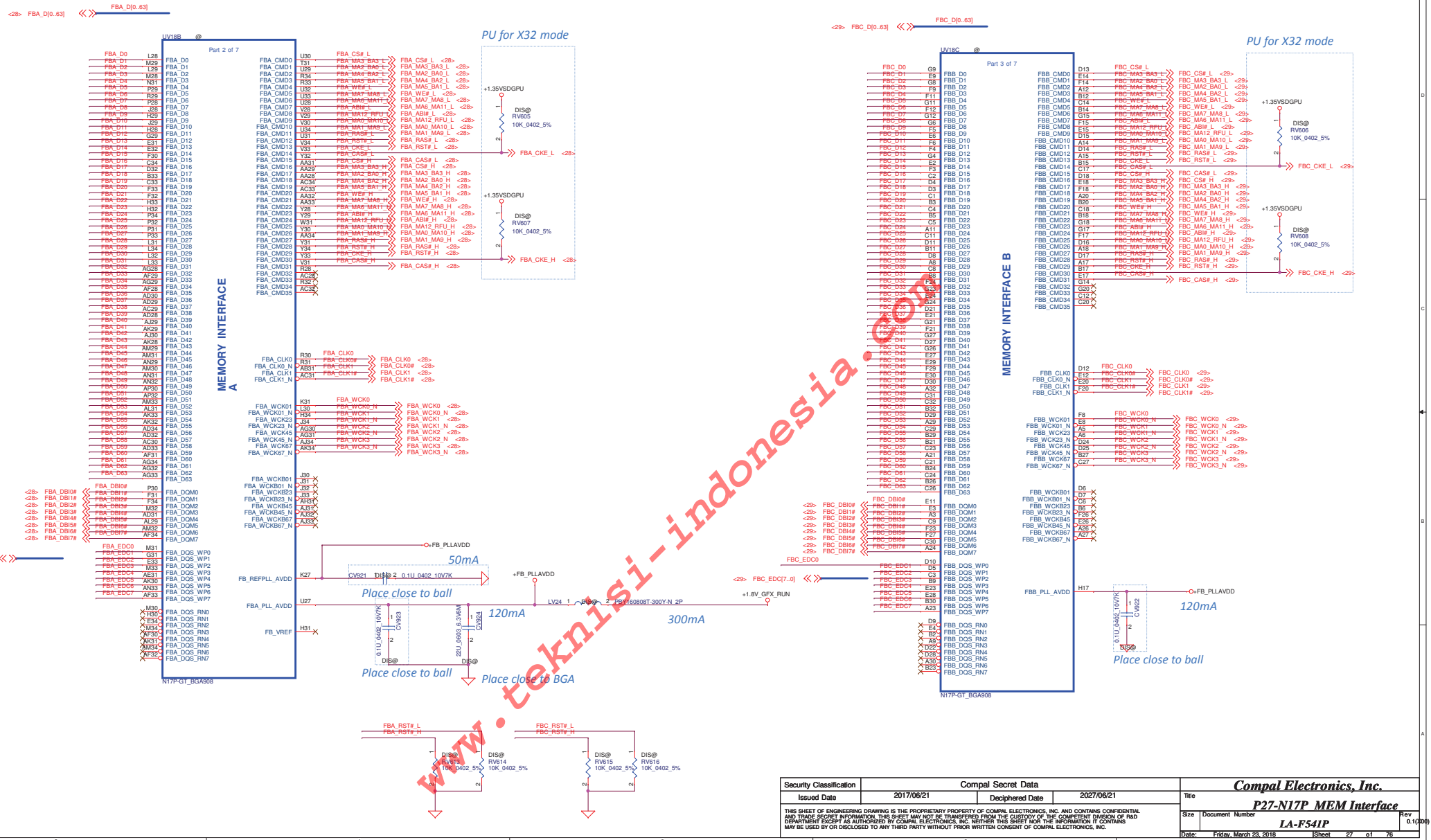


## GPU Power Down Sequence



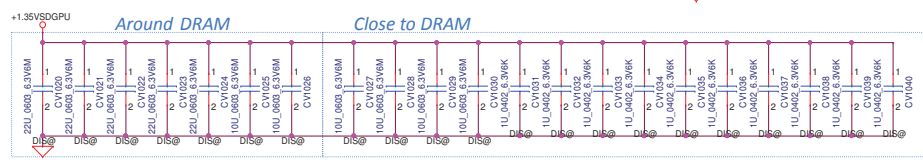
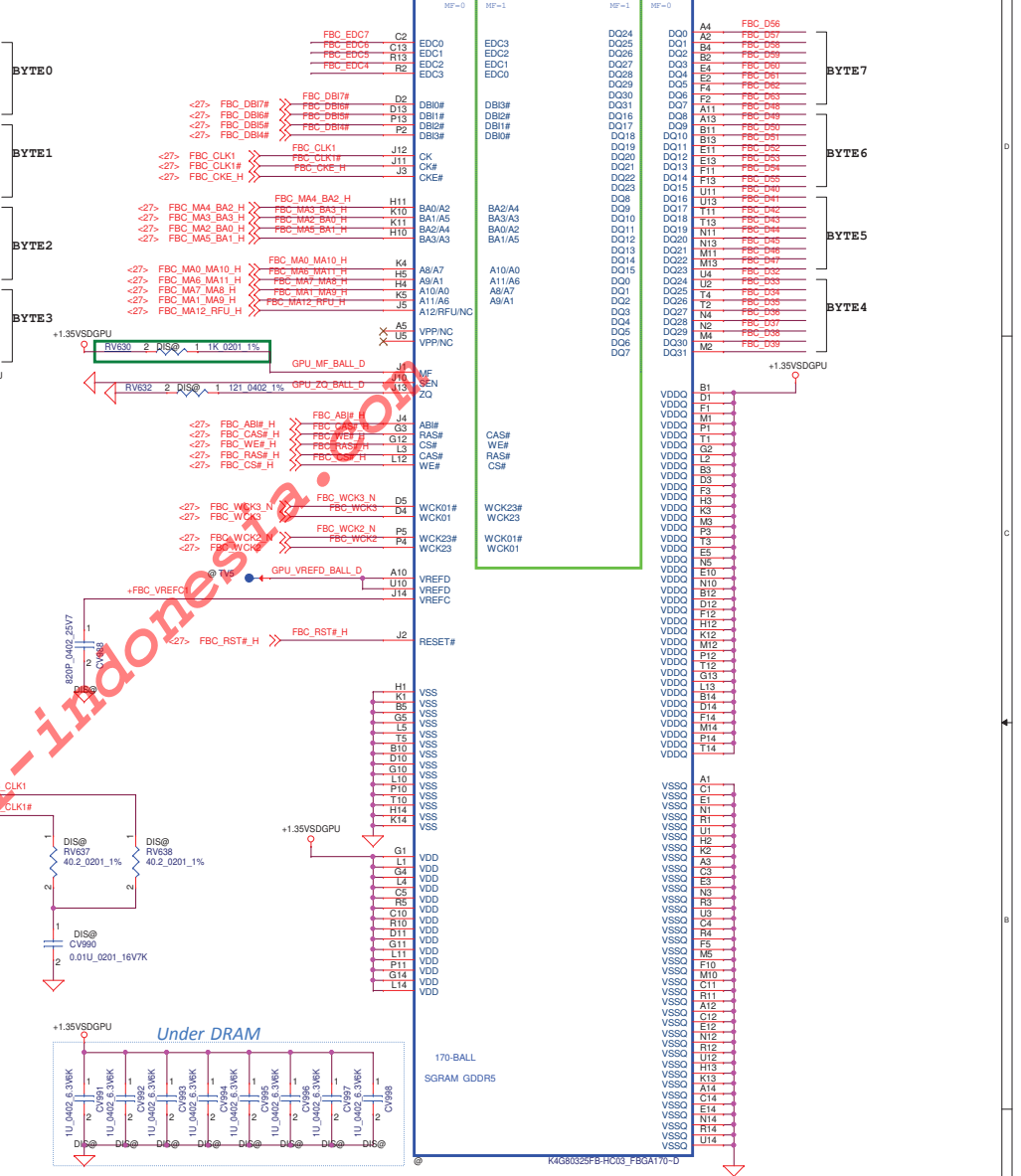
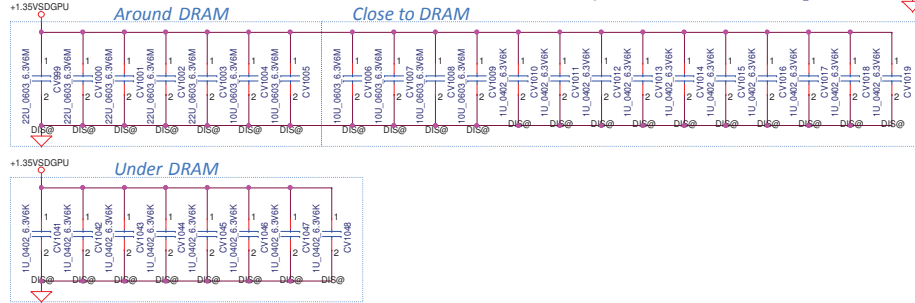
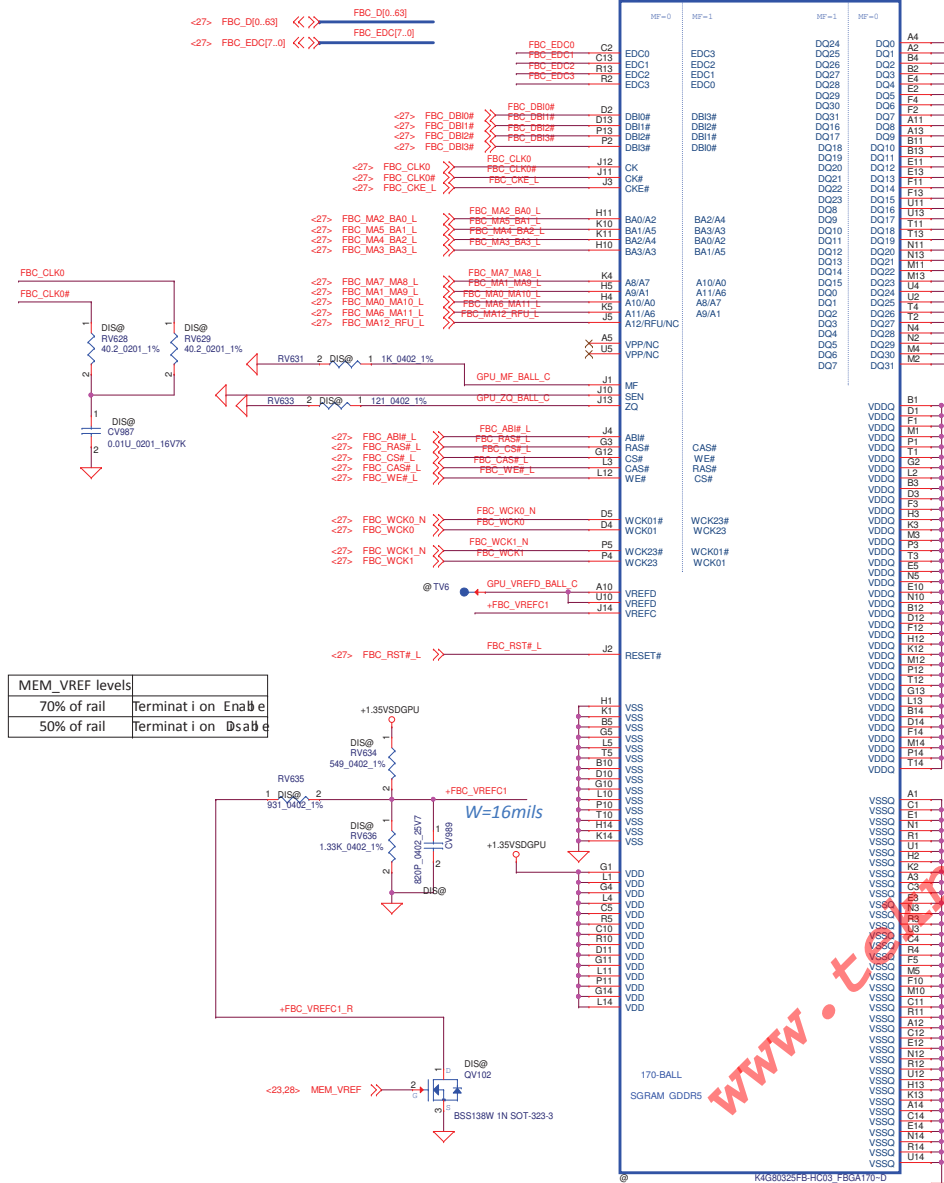
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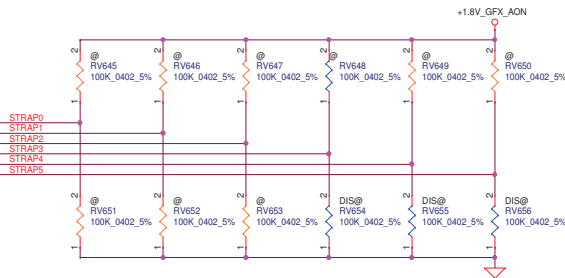
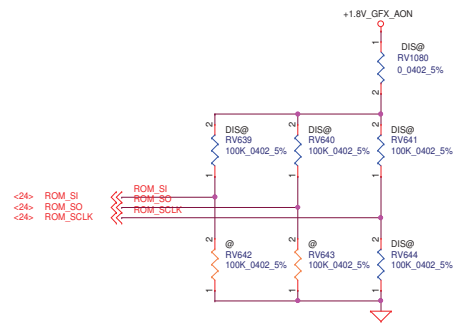






# Memory Partition A- Low 32bit





SMB_ALT_ADDR	State	DEVID_SEL	State	PCIE_CFG	State	VGA_DEVICE	State
Low	Single GPU	Low	Original Device	Low	Normal signal swing	Low	3D Device
High	Dual GPU	High	Re-brand Device ID	High	Reduce the signal amplitude	High	VGA Device

Table 5.5 SMB\_ALT\_ADDR, DEVID\_SEL, PCIE\_CFG, VGA\_DEVICE

Strap Pins <sup>Note 1</sup>			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

Table 5.2 RAMCFG

Strap Pins <sup>see Note</sup>			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	SAMSUNG
L	L	H	1 (0x0001)	MICRON
L	H	L	2 (0x0002)	HYNIX

Table 3. N17P-G0/G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V <sup>2</sup>	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver <sup>1</sup>
			Micron	MT51J256M32HF-70A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver <sup>1</sup>
			Hynix	H5G8H24WJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5G8H24WJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver <sup>1</sup>

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AON and pull-down to GND.			
STRAP2	Do not stuff.			
STRAP3				
STRAP4				

Berlinetta MLK			
Straps	(N17P-Q1)	(N17P-G0)	
Net NAME	state	State	defind
ROM_SCLK	PD 5K	"M"	SOR_EXPOSED(LSB)
ROM_SI	Base on memory RVL	"H"	SOR_EXPOSED
ROM_SO	PD 5K	"H"	SOR_EXPOSED(MSB)
STRAP0	PU 49.9K		RAMCFG(LSB)
STRAP1	Do not stuff		RAMCFG
STRAP2	Do not stuff		RAMCFG(MSB)
STRAP3	Do not stuff	"L"	SMB_ALT_ADDR(0), DEVID_SEL(0)
STRAP4	Do not stuff	"L"	PCIE_CFG(0), VGA_DEVICE(0)
STRAP5	Unused	"L"	

Table 4. N17P-Q1 GDDR5 Recommended Memories

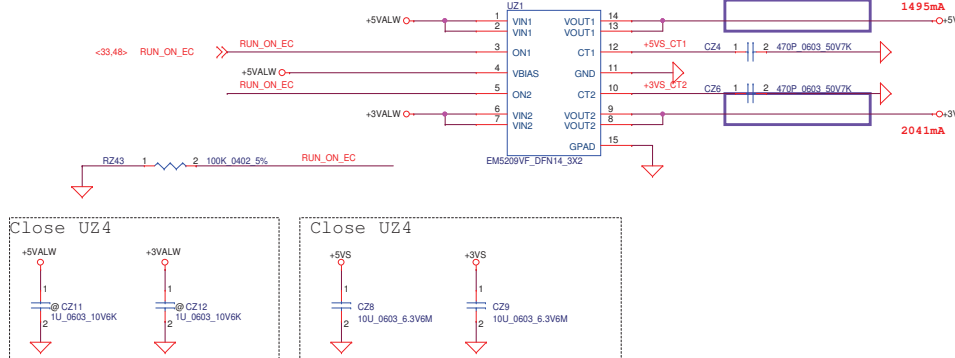
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V	Samsung	K4G80325FB-HC03	B-die	0x8	6 Gbps	N/A	Full	Production candidate
			Micron	MT51J256M32HF-60A	A-die	0x9	6 Gbps	N/A	Full	Production candidate

Notes:

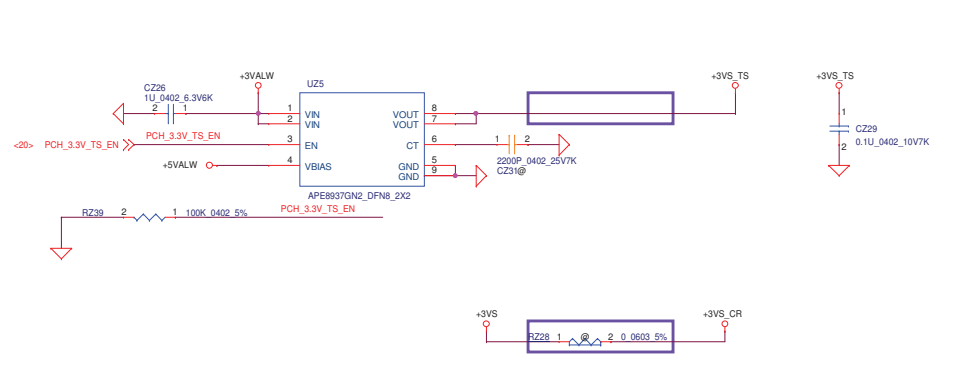
1. For N17P-Q1, the maximum allowable memory case temperature is 85 °C.



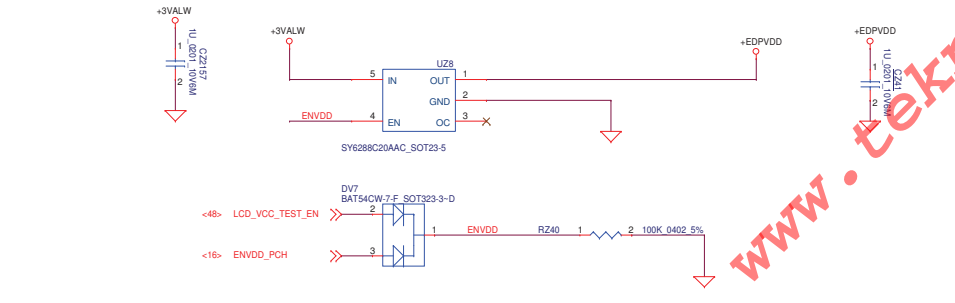
**+5VALW to +5VS  
+3VALW to +3VS**



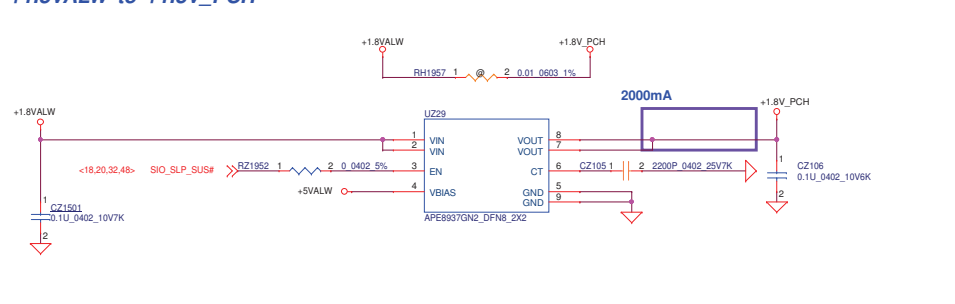
**Touch Screen Load Switch & Card Reader**



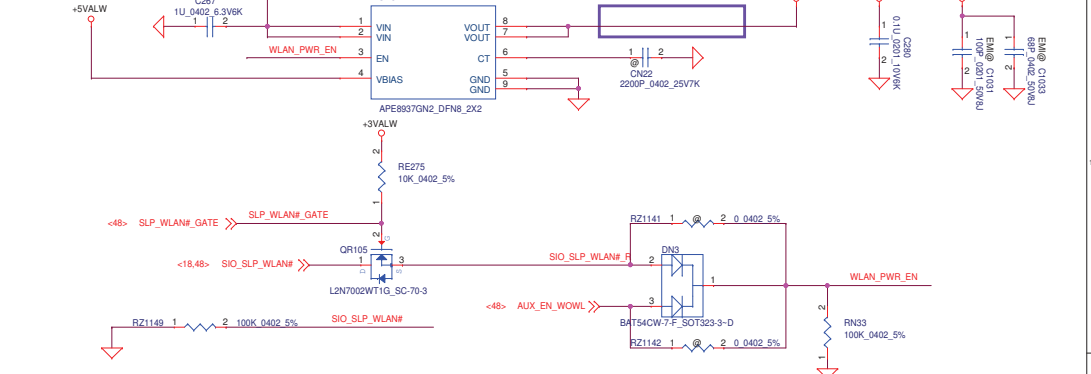
**eDP & Camera Load Switch**



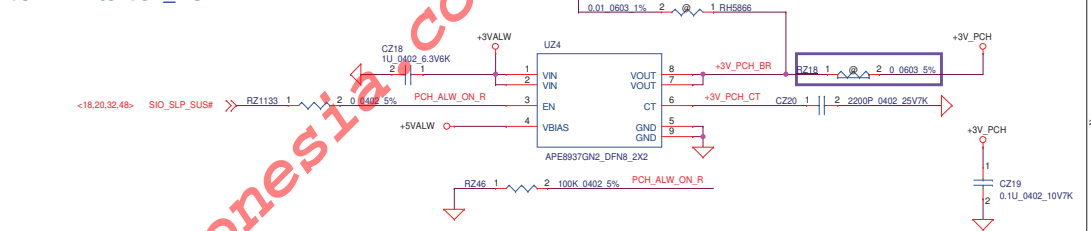
**+1.8VALW to +1.8V\_PCH**



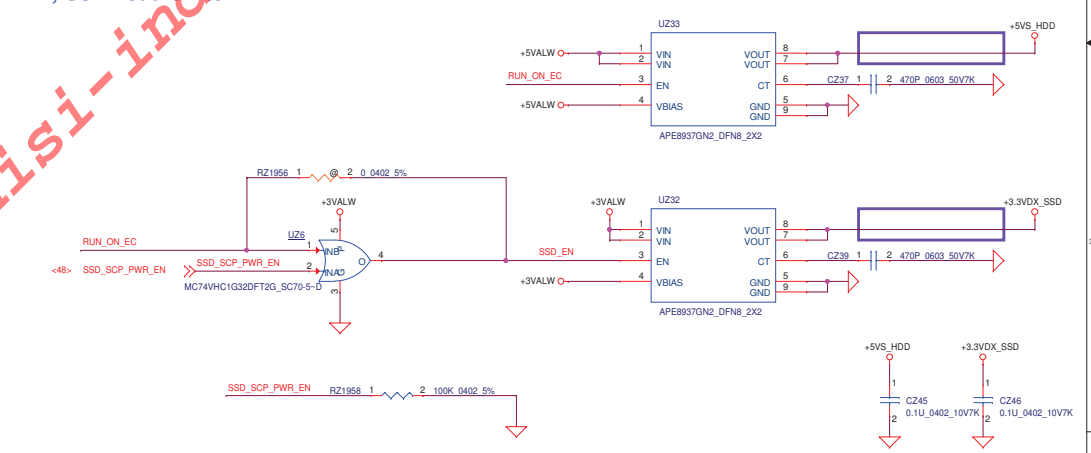
**WLAN Load Switch**



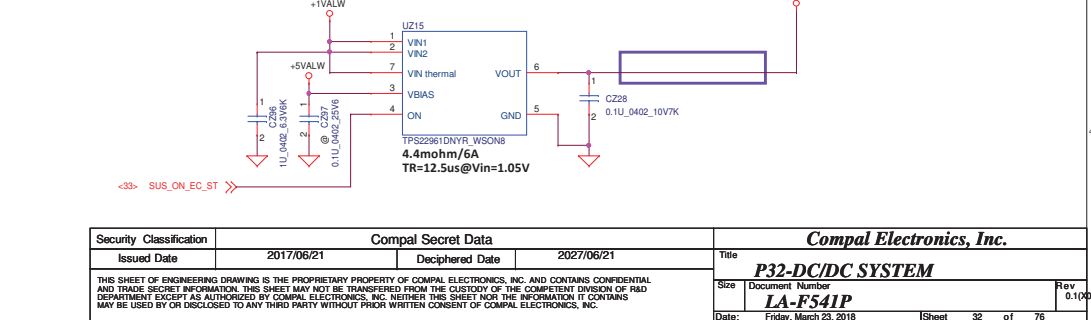
**+3VALW to +3V\_PCH**



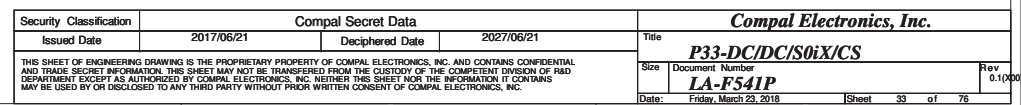
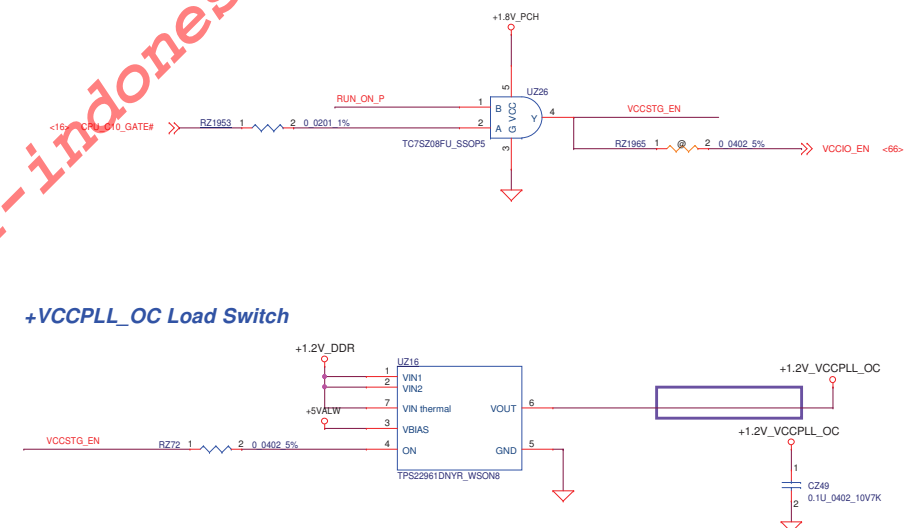
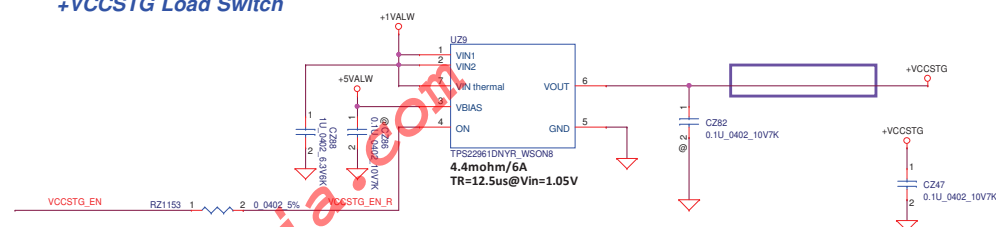
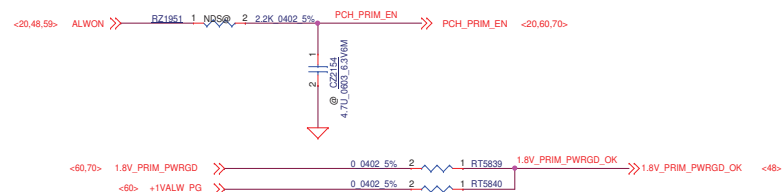
**HDD, SSD Load Switch**



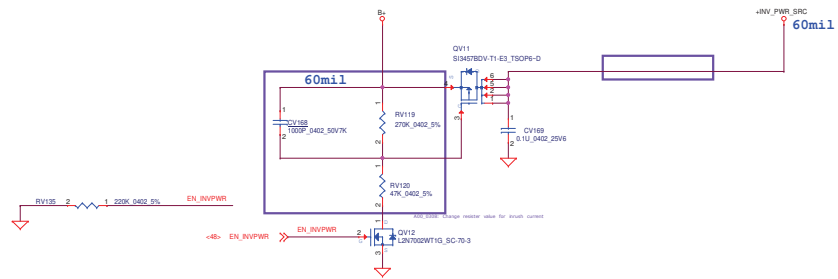
**+VCCST Load Switch**



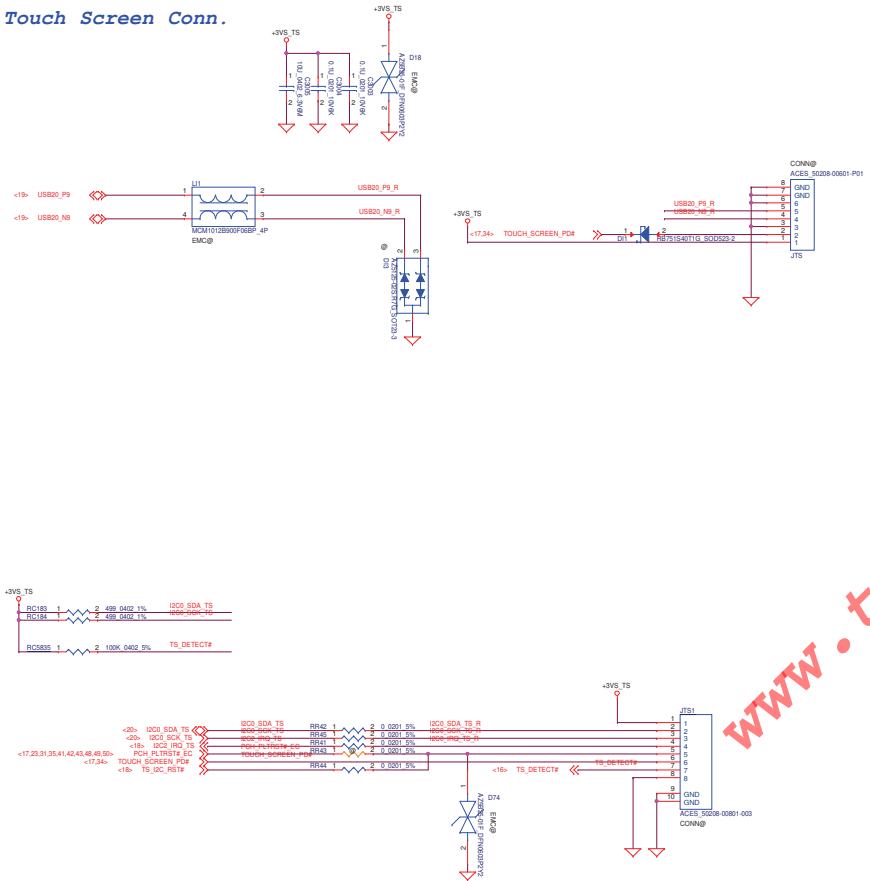
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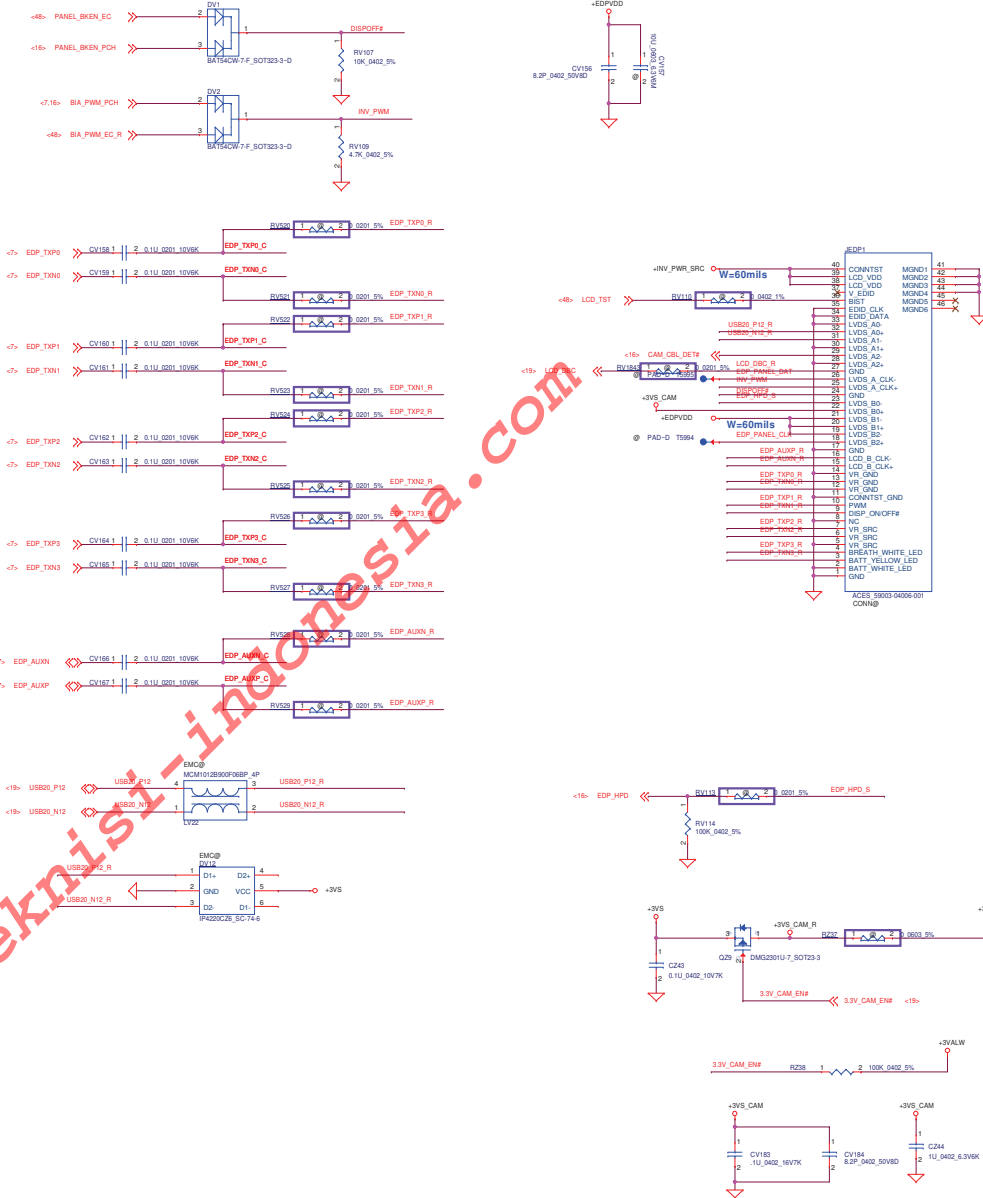
LCD backlight PWR CTRL



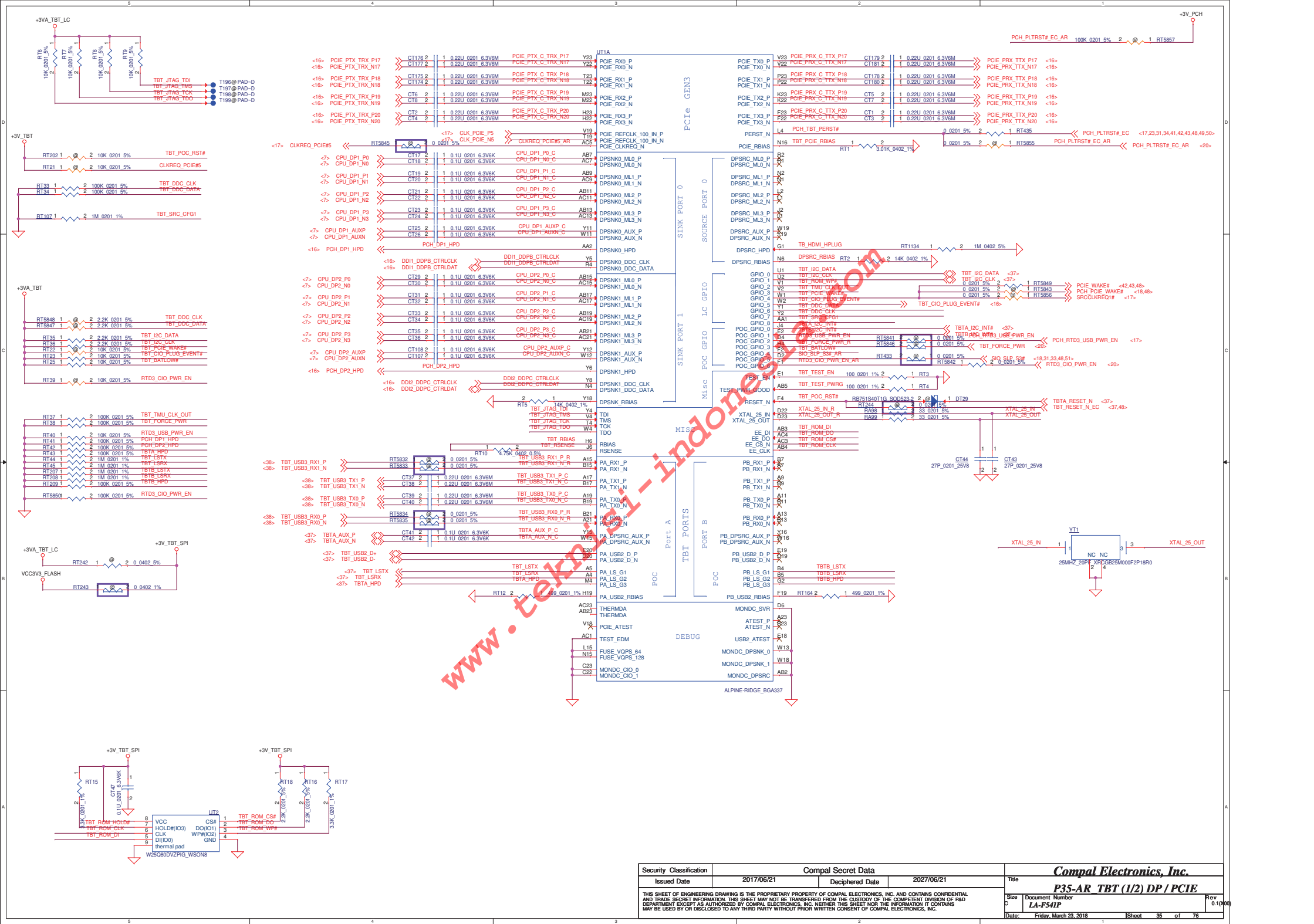
*Touch Screen Conn.*



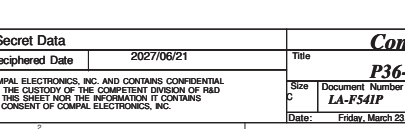
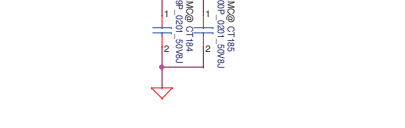
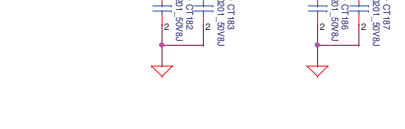
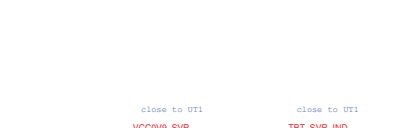
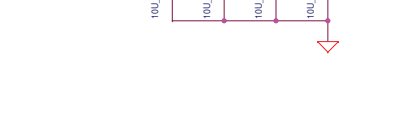
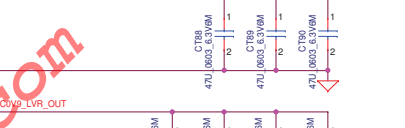
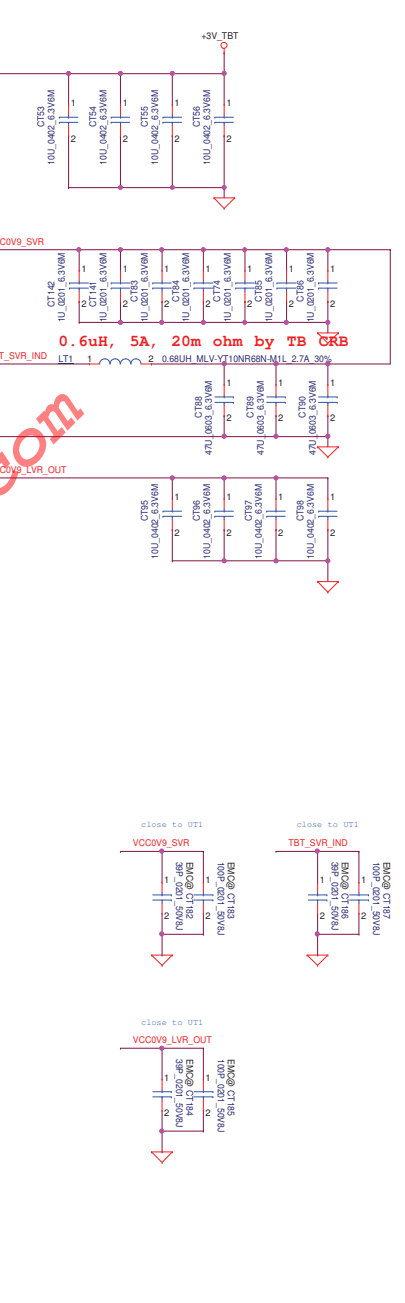
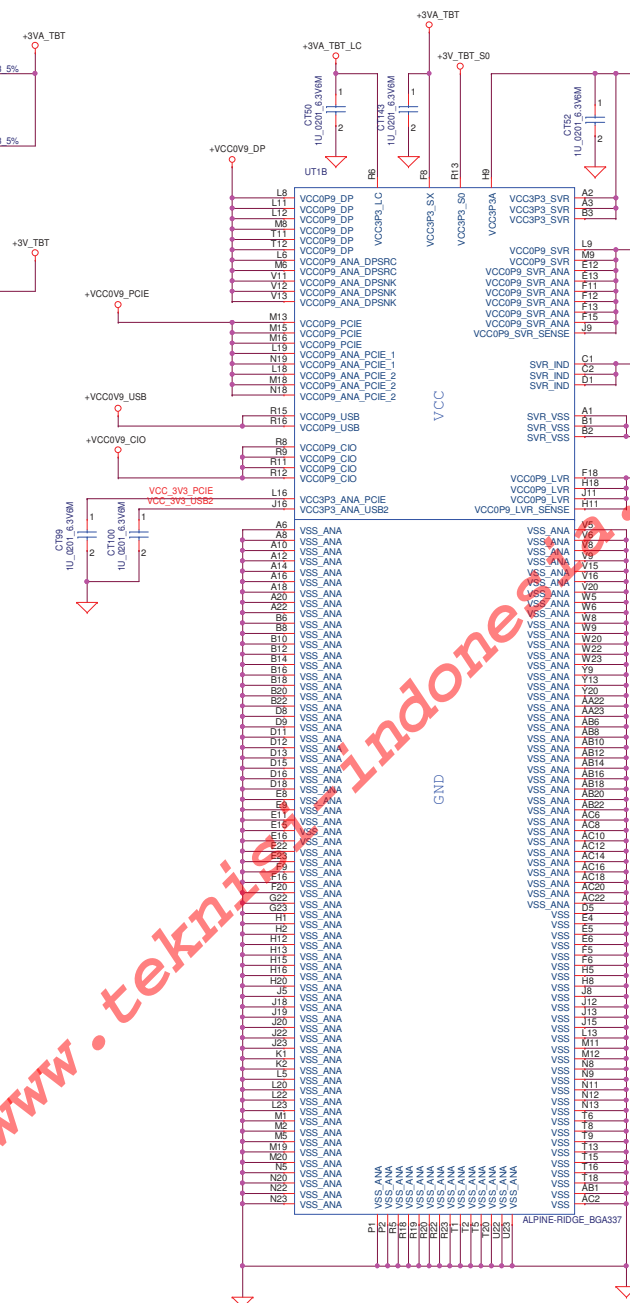
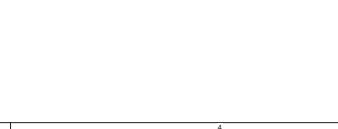
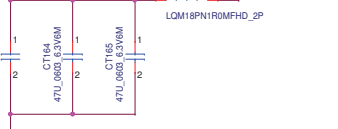
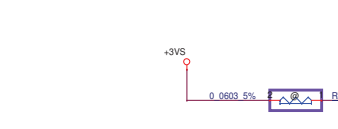
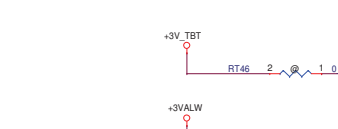
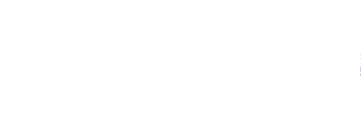
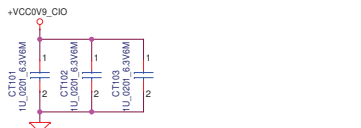
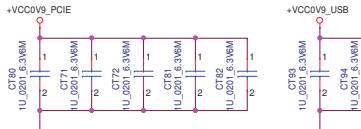
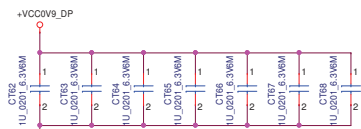
***eDP & CCD(RGB) Conn.***



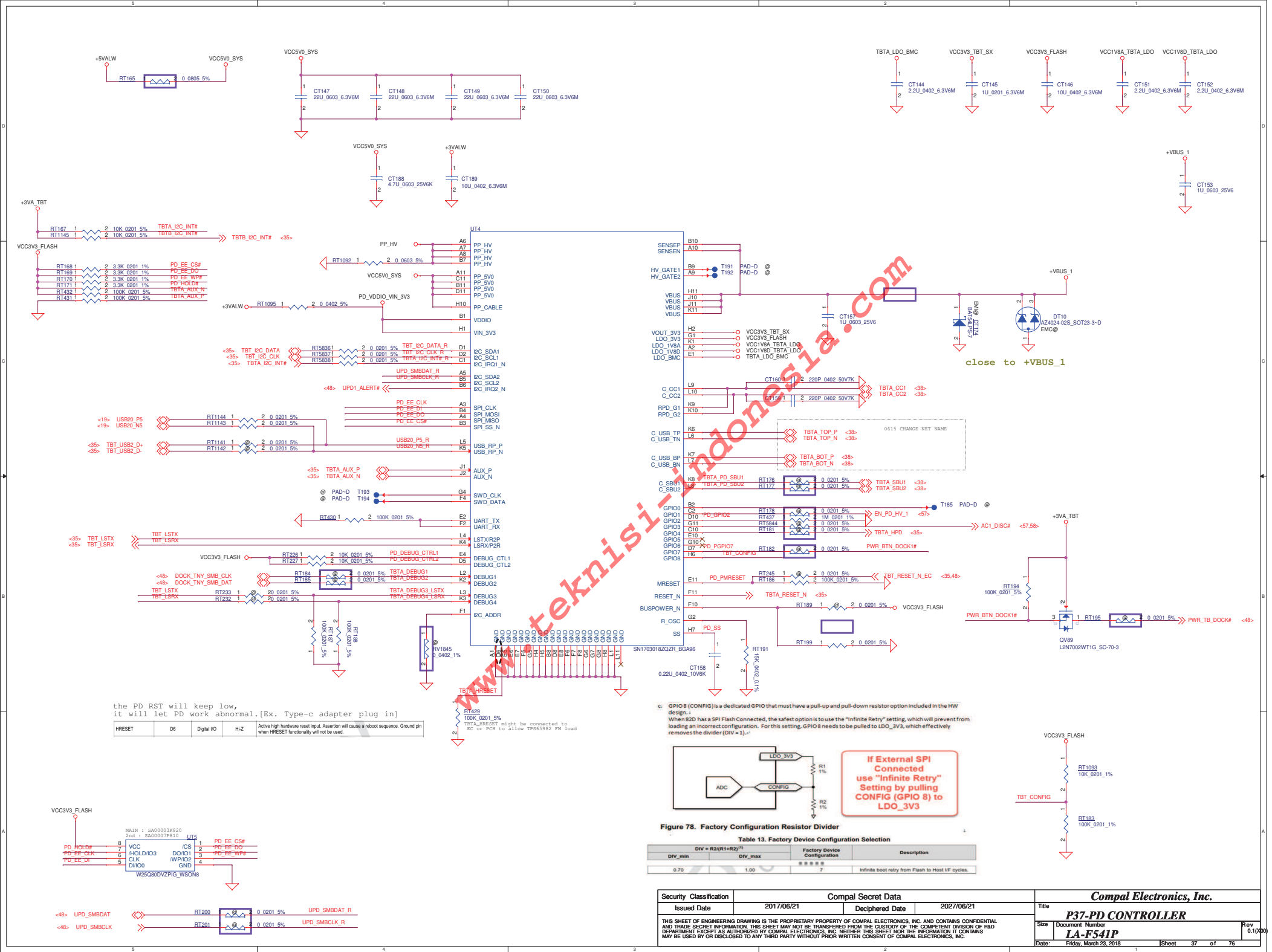
Security Classification	Compul Secret Data		Title		Compul Electronics, Inc.	
Issued Date	2017/06/21	Deciphered Date	2027/06/21	Item	P34-CDP/CDT/TS	
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				Date	15-F541P	
				Date	Friday, March 24, 2018	
				Sheet	34 of 76	

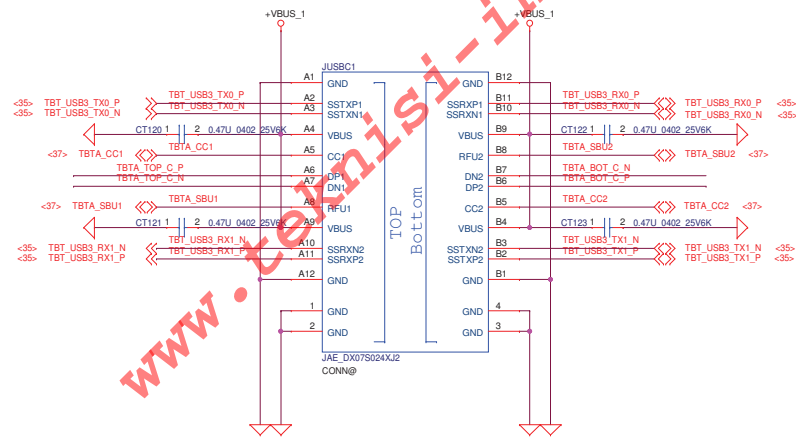
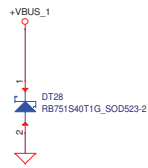
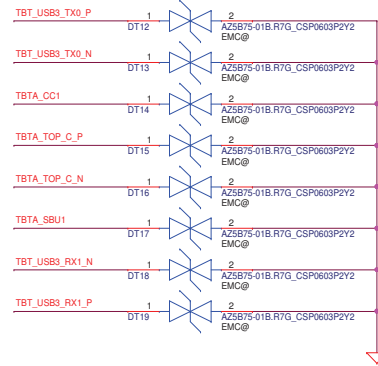
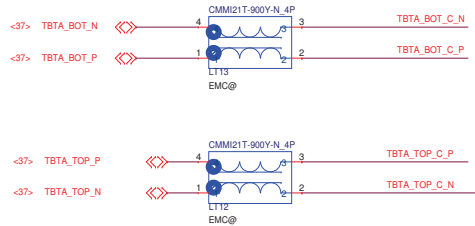


Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b> <b>P35-AR TBT (1/2) DP / PCIE</b>		
Issued Date	2017/06/21	Deciphered Date	2027/06/21	Title		
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				Date:	Friday, March 23, 2018	Sheet 35 of 76

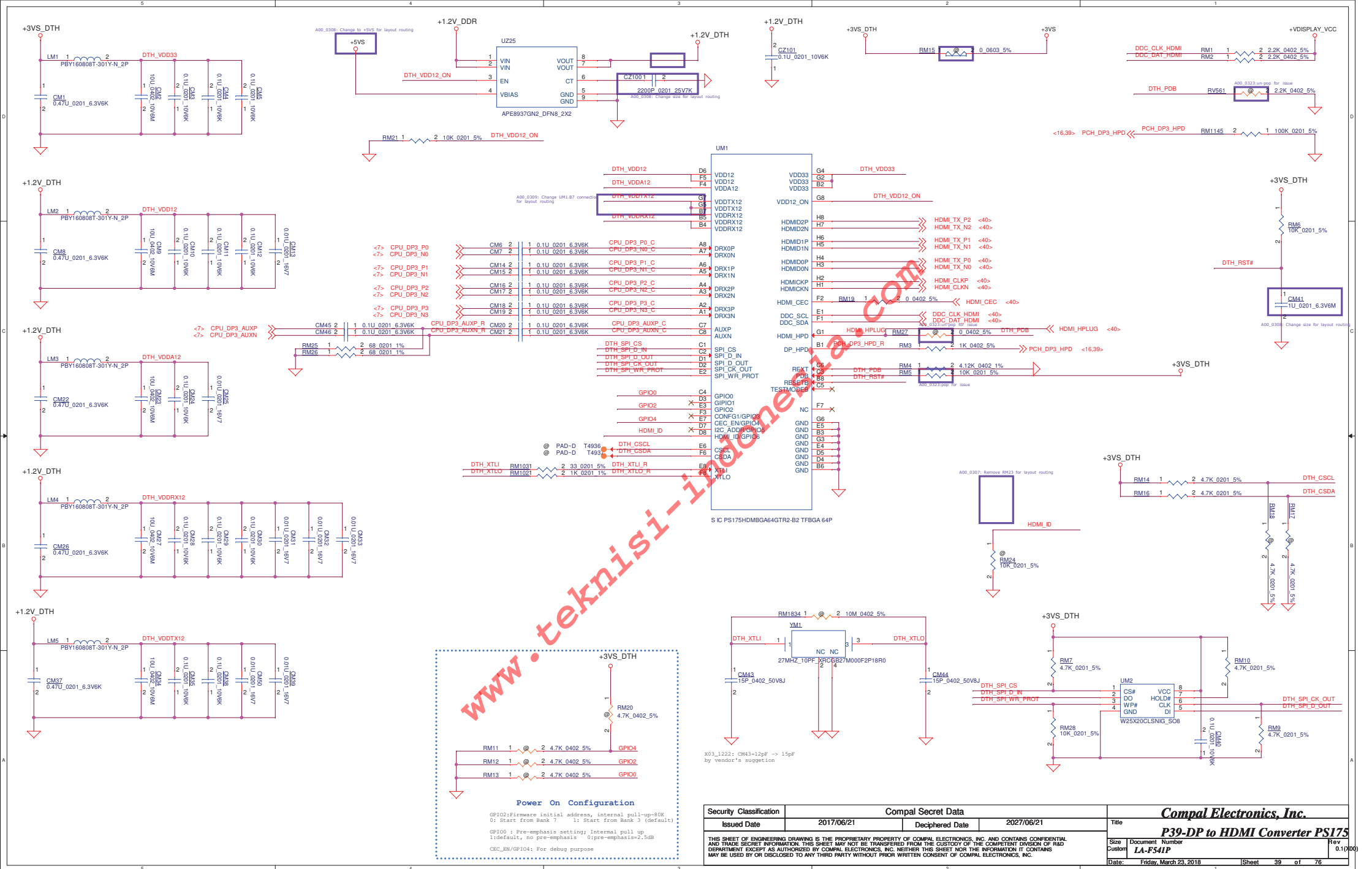


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/06/21	Deciphered Date	2027/06/21	Title
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Size	Document Number	Sheet	36	Rev 0.1(00)
Date:	Friday, March 23, 2018	Sheet	36	of 76

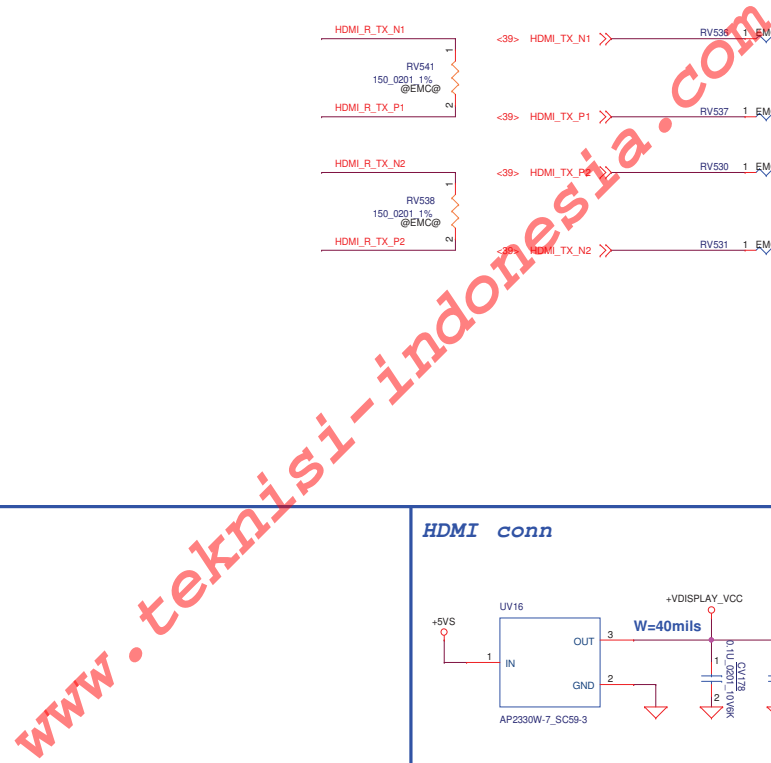




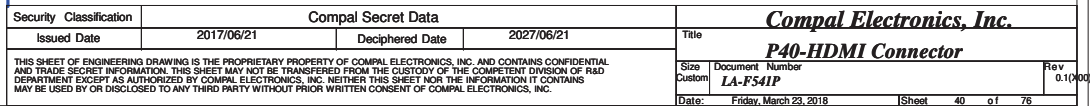
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Issued Date	2017/06/21	Deciphered Date	2027/06/21	Title
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Size	Document Number	Rev		0.1(00)
D	LA-FS41P	Date: Wednesday, March 28, 2018		Sheet 38 of 76



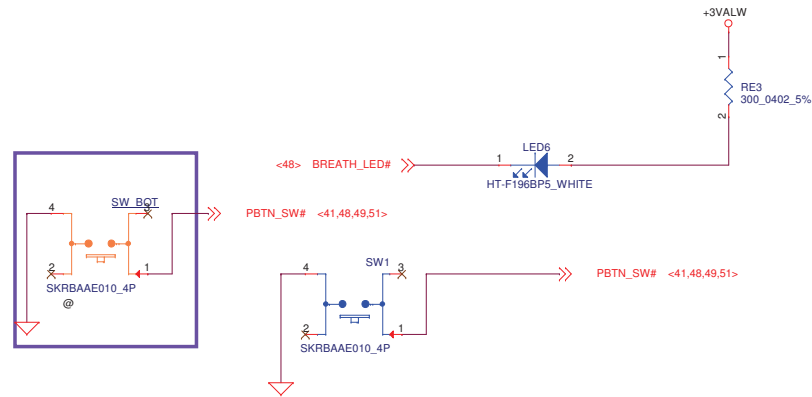
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>P39-DP to HDMI Converter PS175</b>	
Issued Date	2017/06/21	Deciphered Date	2027/06/21	Title	
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				Document Number	01(000)
				LA-F541P	
Date:	Friday, March 23, 2018	Sheet	39	of	76



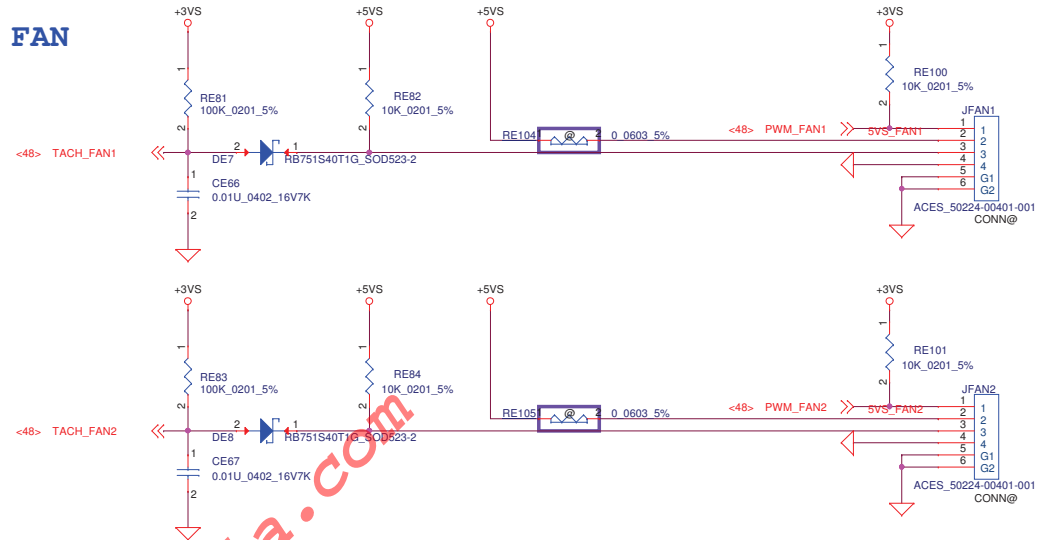
## HDMI conn



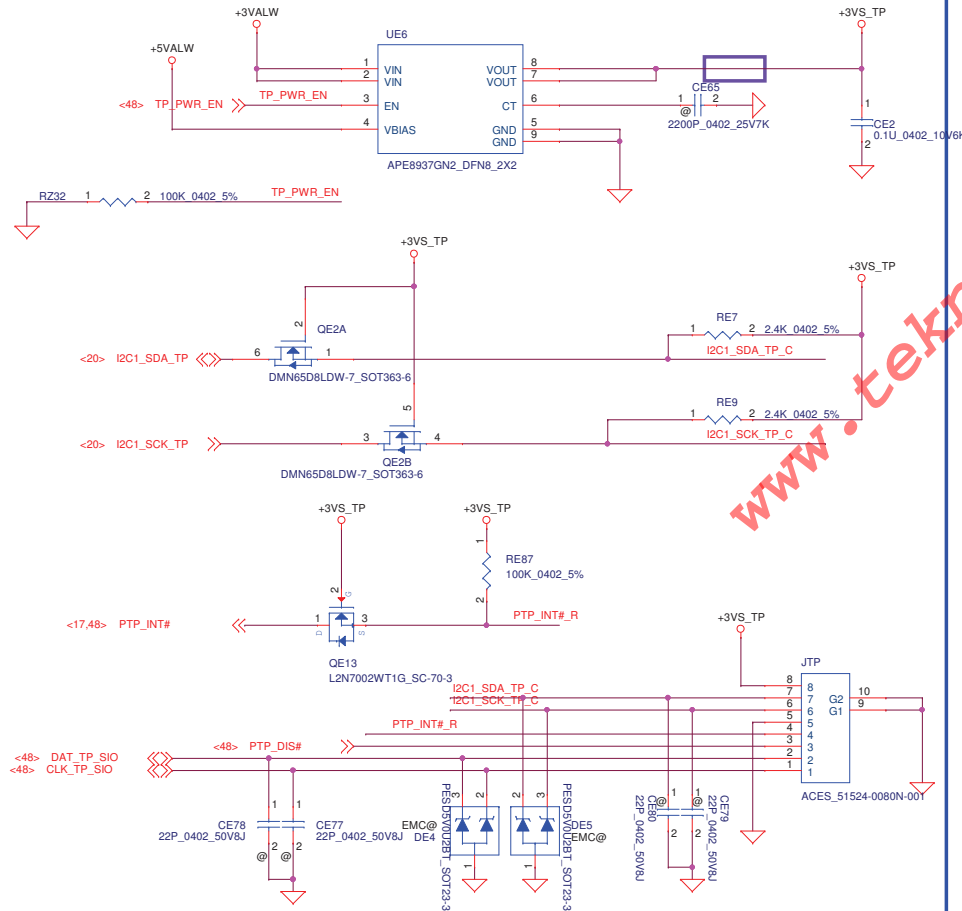
Power Button and LED



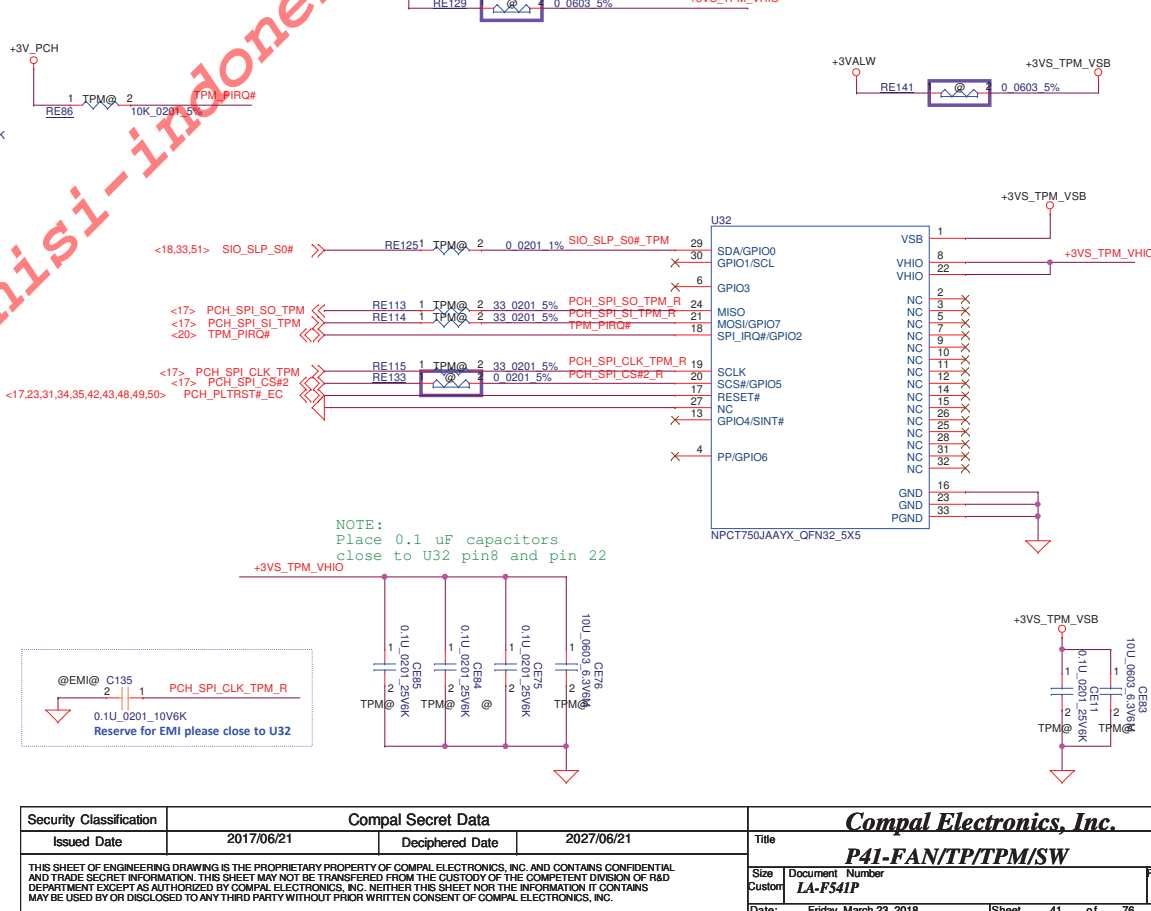
PWM FAN



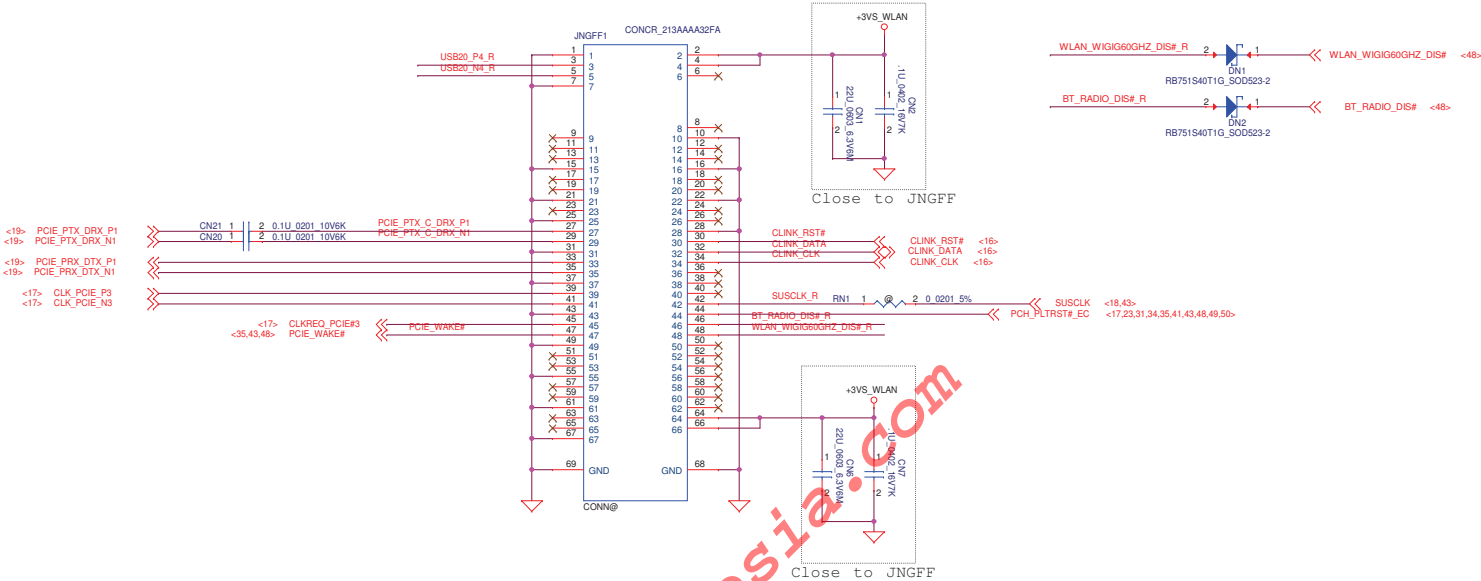
Touch pad



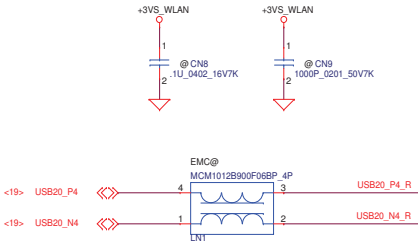
Nuvoton TPM



M.2 Slot-A Key-A (WLAN + BT)



Reserve for EMI

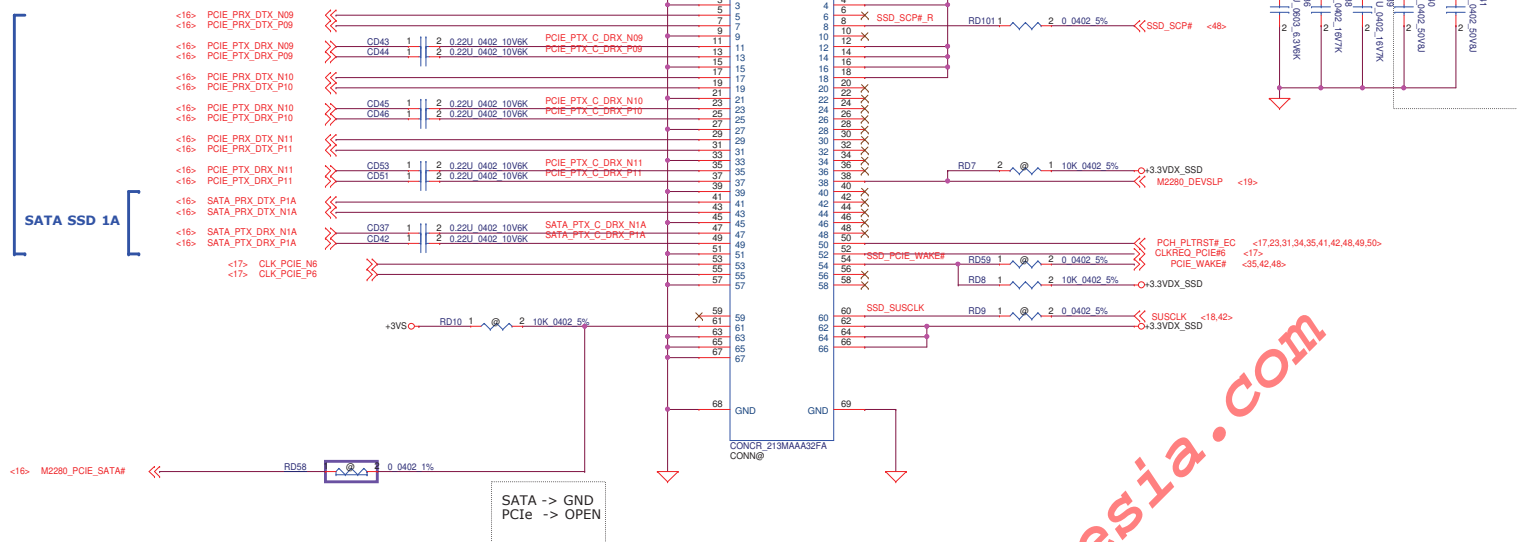


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/06/21	Deciphered Date	2027/06/21	Title
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Size	Document Number	Rev		0.1000
D	LA-F541P	Date: Friday, March 23, 2018		Sheet 42 of 76

# M.2 Slot-C Key-M (SSD)

PCIe SSD

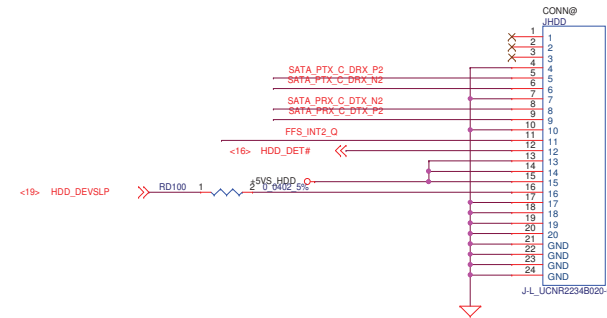
SATA SSD 1A



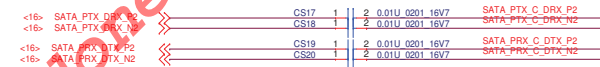
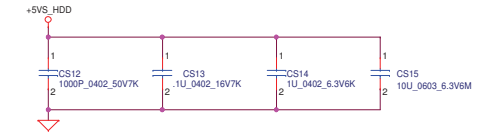
www.teknisi-indonesia.com

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Size	Document Number	Rev		0.1000	
C	LA-FS41P				
Date:	Friday, March 23, 2018	Sheet	43	of	76

## HDD CONN

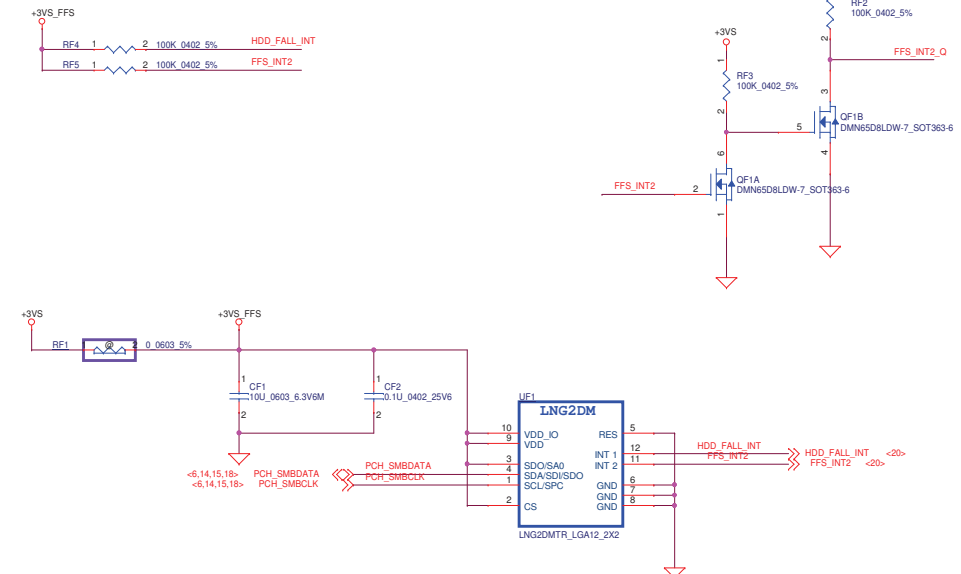


Place near HDD CONN (JHDD1)



## BYPASS Circuit

## Free Fall Sensor

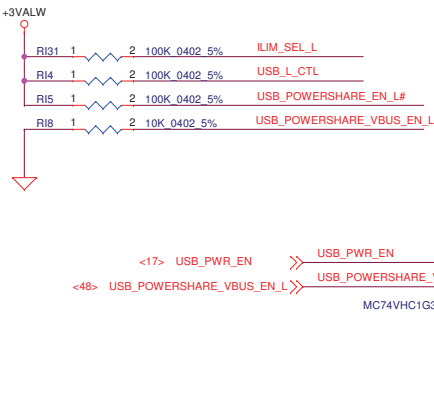
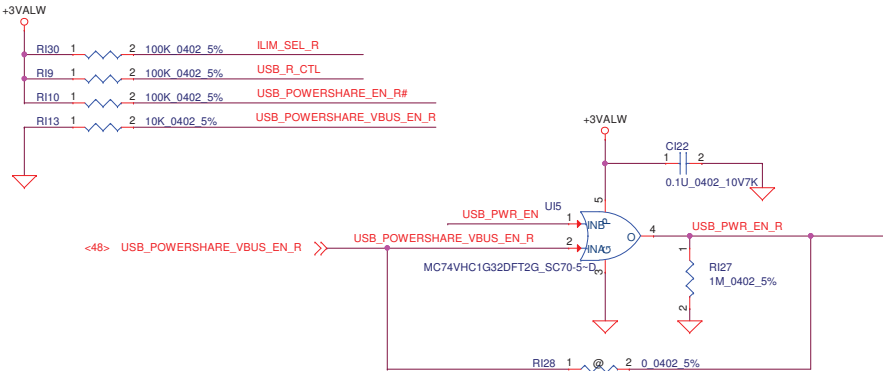


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/06/21	Deciphered Date	2027/06/21	Title
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				Document Number
				LA-FS41P
				Rev
				0.1000
				Date: Friday, March 23, 2018
				Sheet 44 of 76

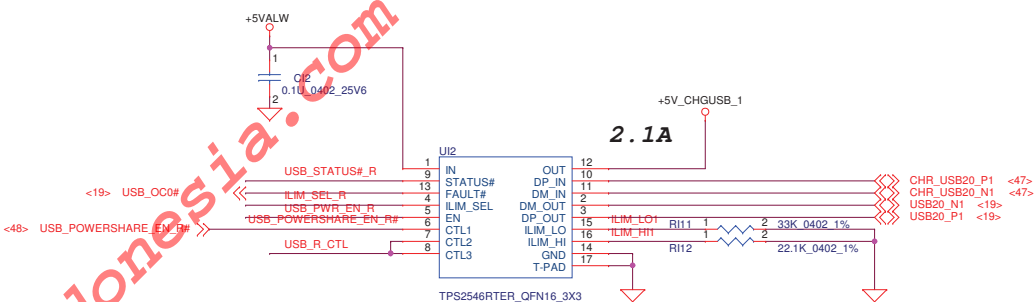
USB Powershare

Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

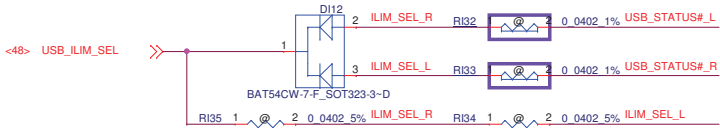
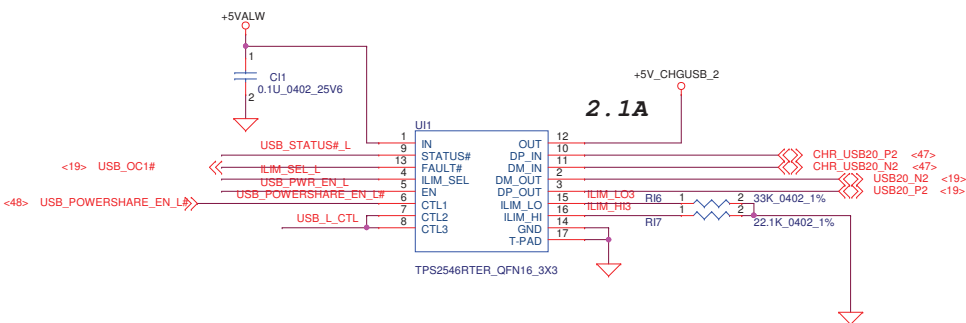
Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)

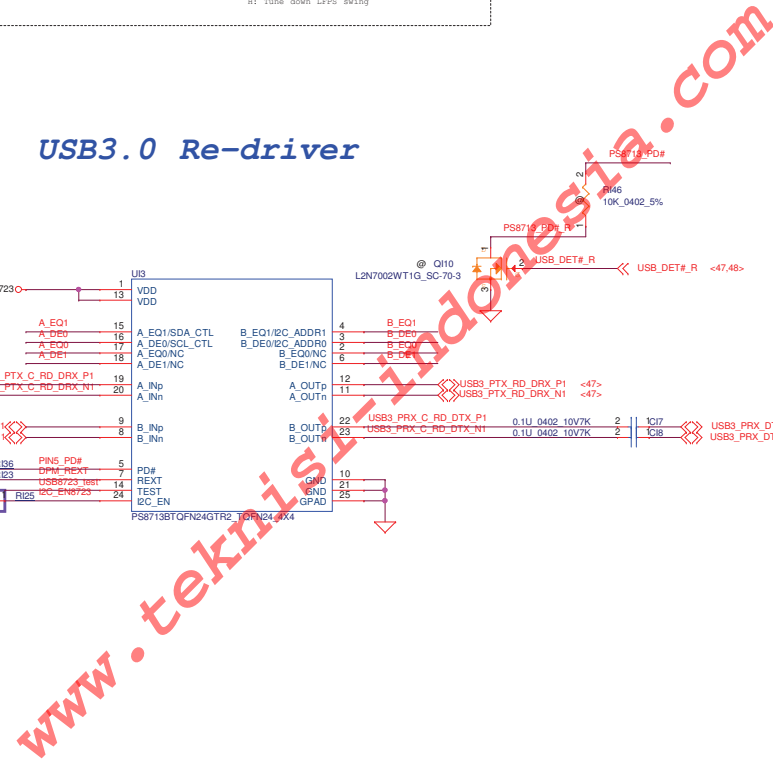


USB3.1 / USB2.0 Port1 (Right Side)



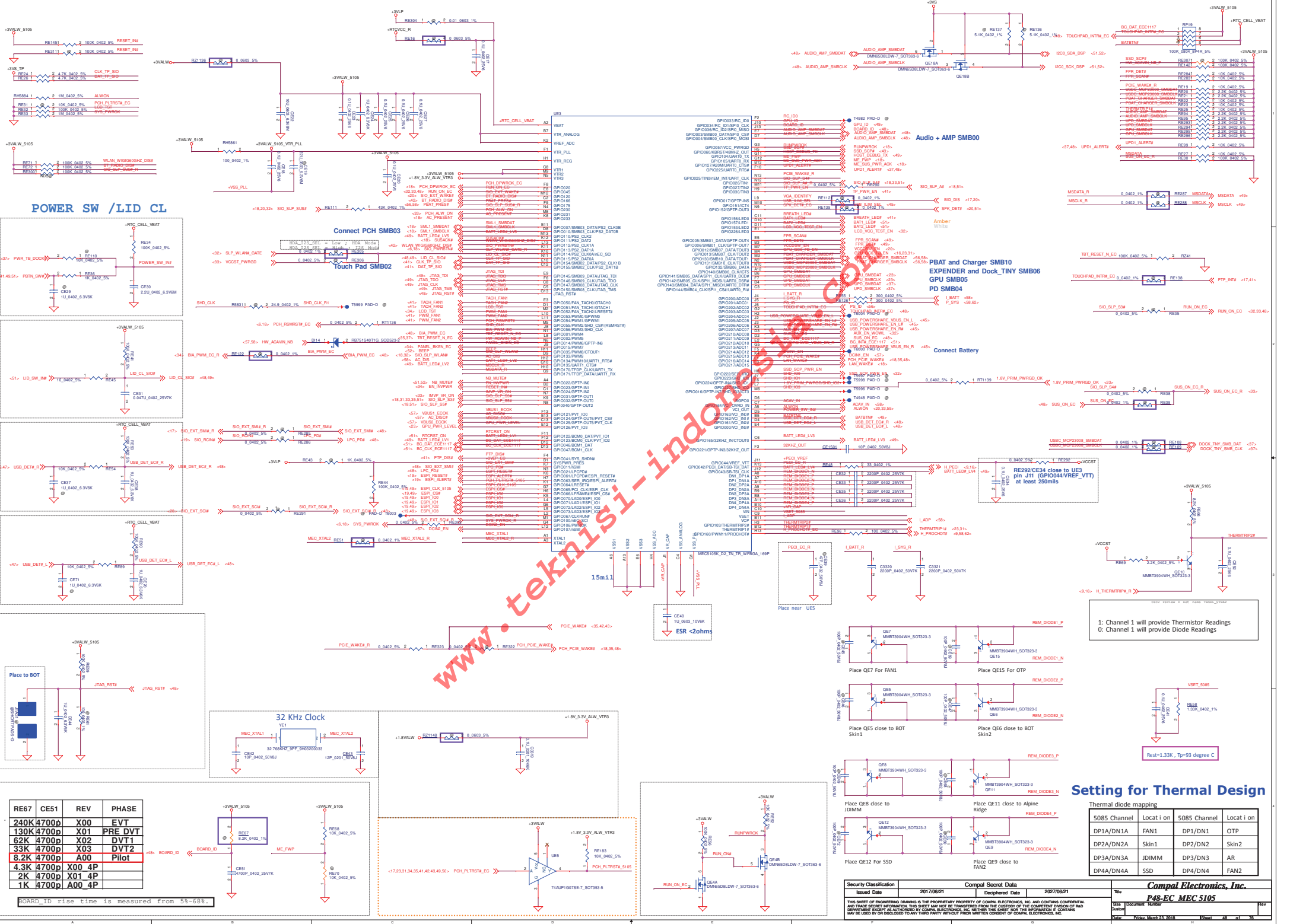
USB3.1 / USB2.0 Port2 (Left Side)



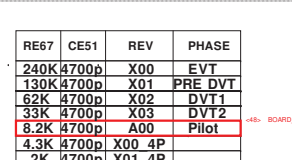
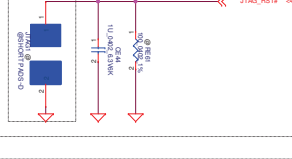
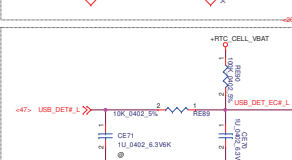
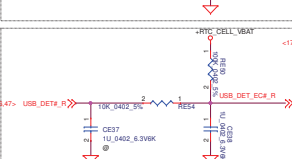
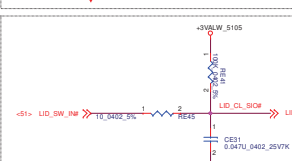
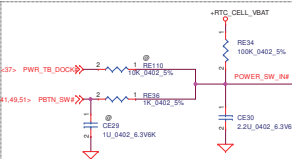


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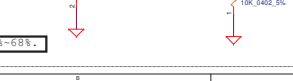
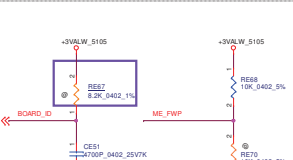
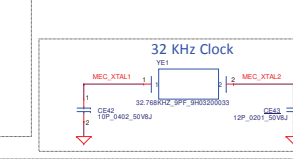
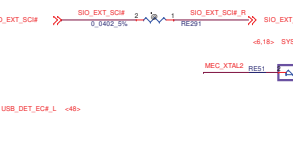
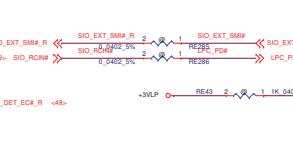
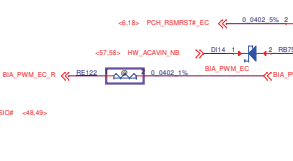
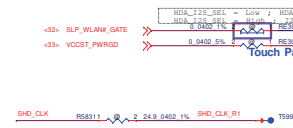
POWER SW /LID CL



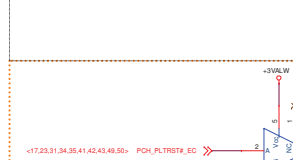
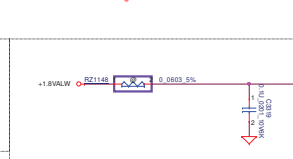
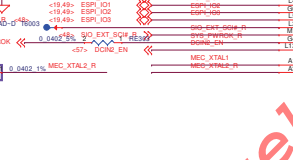
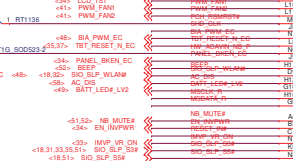
RE67	CE51	REV	PHASE
240K 4700p	X00	EVT	
130K 4700p	X01	PRE DVT	
62K 4700p	X02	DVT1	
33K 4700p	X03	DVT2	
8.2K 4700p	A00	Pilot	
4.3K 4700p	X00_4P		
2K 4700p	X01_4P		
1K 4700p	A00_4P		

BOARD\_ID rise time is measured from 5%-68%.

Connect PCH SMB03



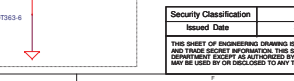
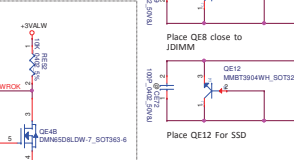
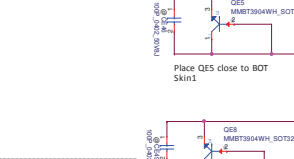
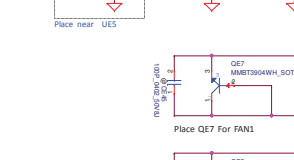
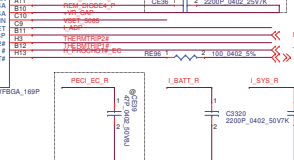
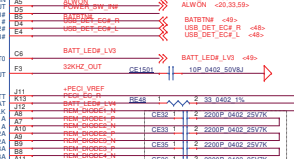
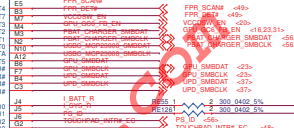
Touch Pad SMB02



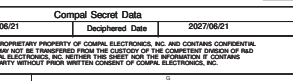
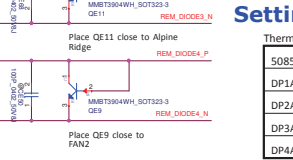
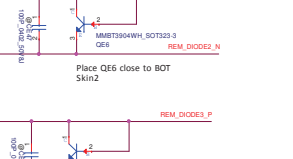
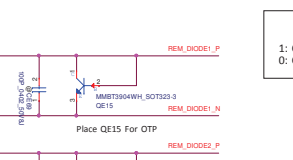
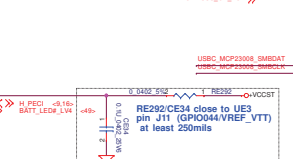
Audio + AMP SMB00



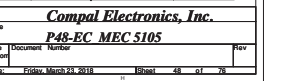
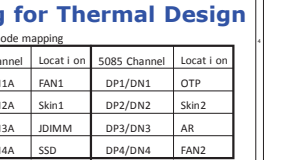
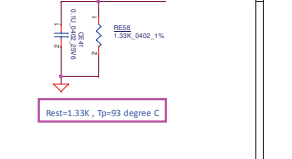
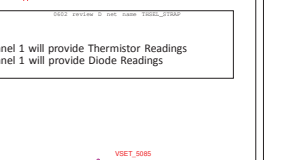
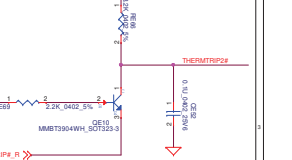
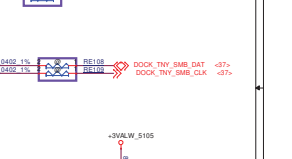
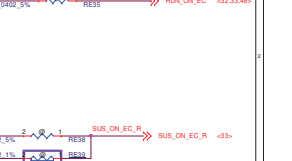
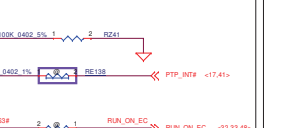
PBAT and Charger SMB10



EXPENDER and Dock TINY SMB06



Connect Battery



Setting for Thermal Design

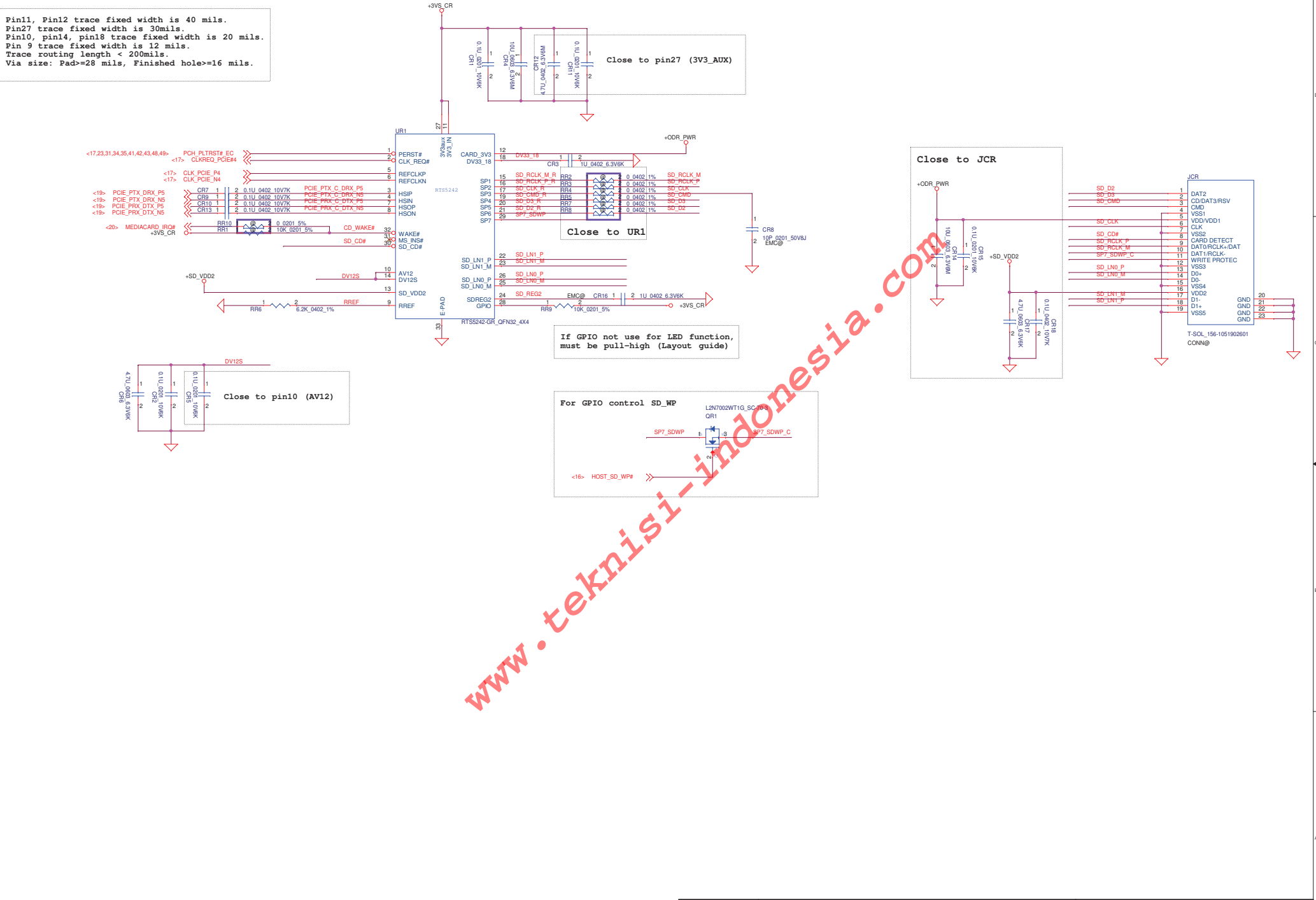
5085 Channel	Locat i on	5085 Channel	Locat i on
DP1A/DN1A	FAN1	DP1/DN1	OTP
DP2A/DN2A	Skin1	DP2/DN2	Skin2
DP3A/DN3A	JDImm	DP3/DN3	AR
DP4A/DN4A	SSD	DP4/DN4	FAN2

Thermal diode mapping

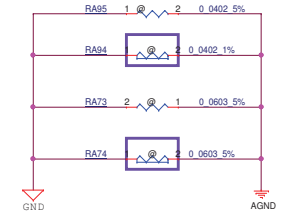
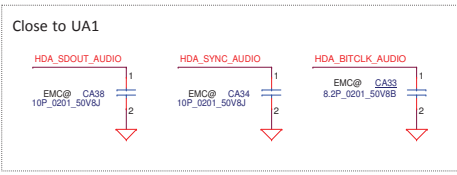
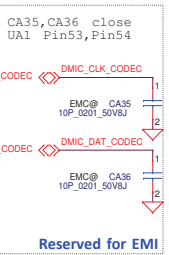
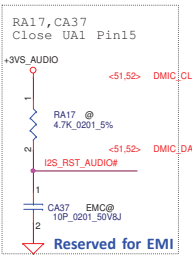
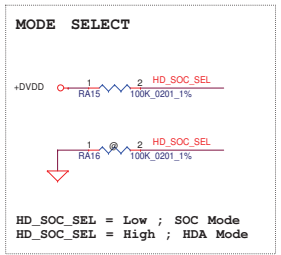
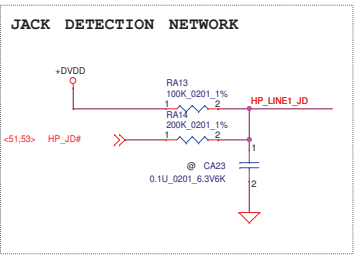
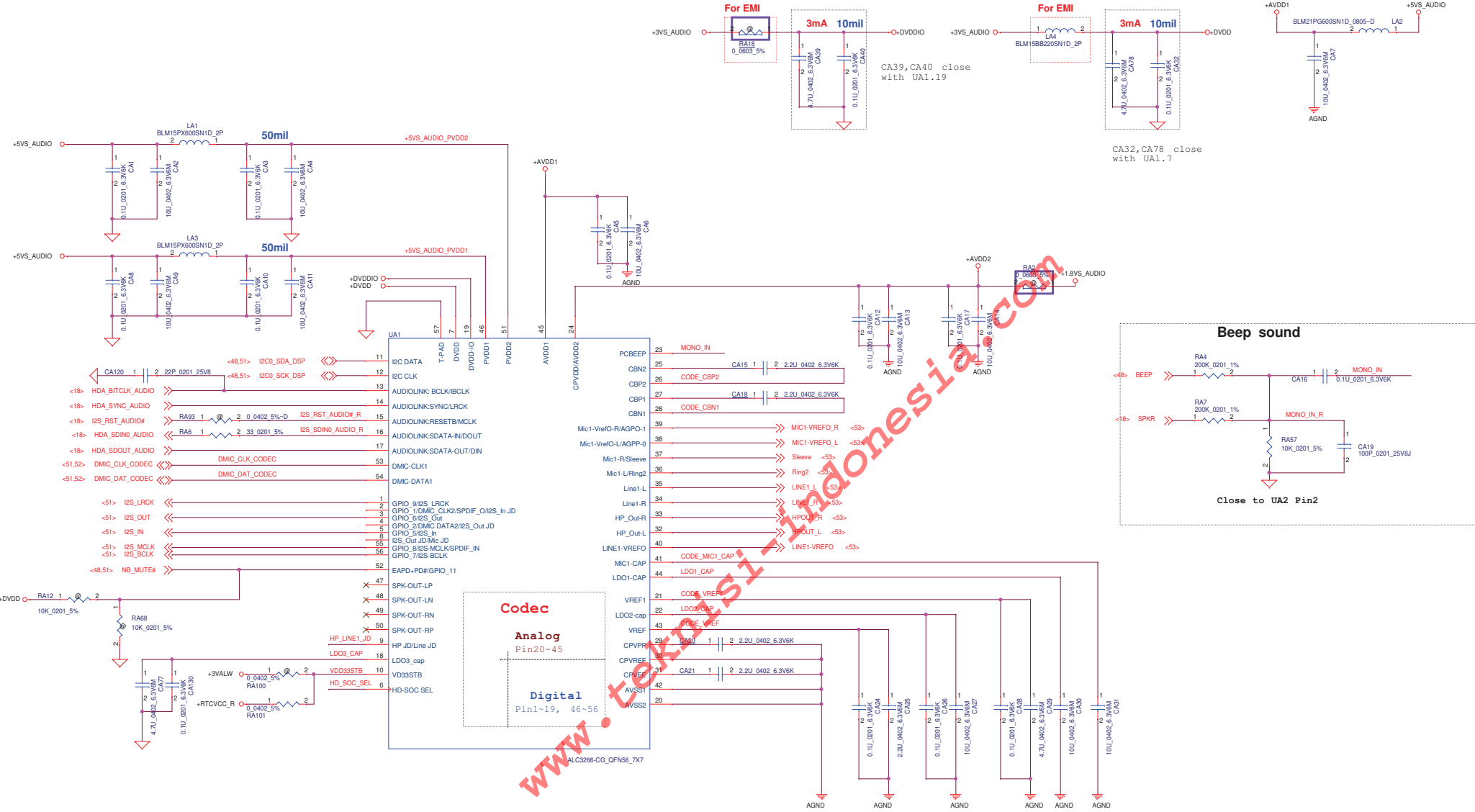


Card Reader

Pin11, Pin12 trace fixed width is 40 mils.  
Pin27 trace fixed width is 30mils.  
Pin10, pin14, pin18 trace fixed width is 20 mils.  
Pin 9 trace fixed width is 12 mils.  
Trace routing length < 200mils.  
Via size: Pad>=28 mils, Finished hole>=16 mils.

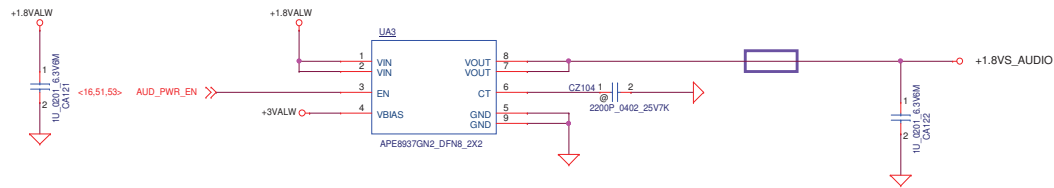




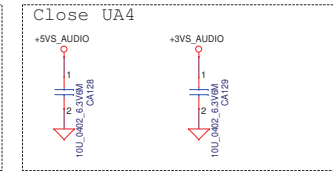
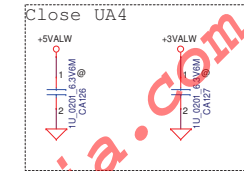
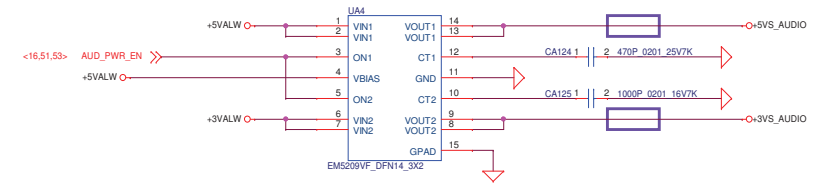


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				LA-F541P	Rev 0.1(000)
				Date:	Friday, March 23, 2018
				Sheet	52 of 76

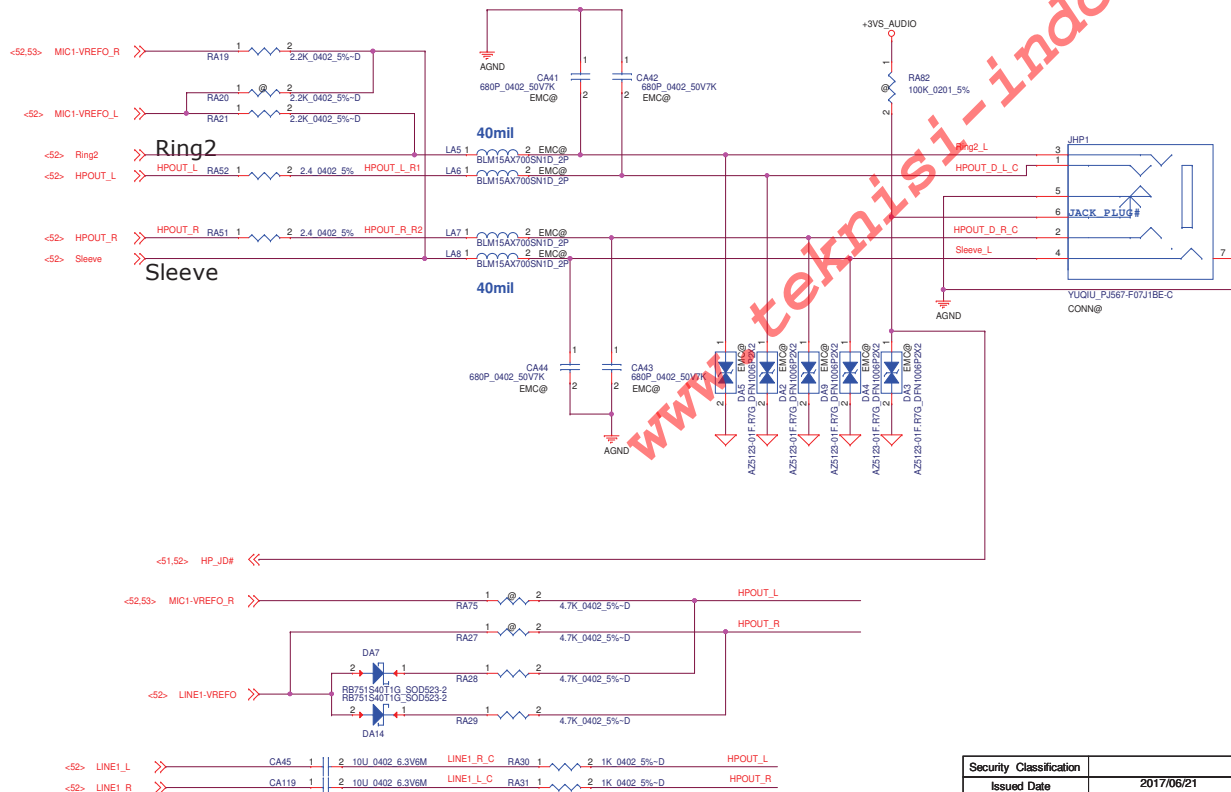
## +1.8VALW To +1.8VS\_AUDIO



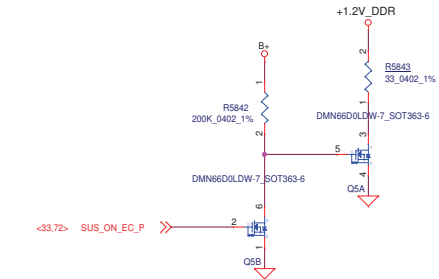
## +5VALW and +3VALW To +5VS\_AUDIO and +3VS\_AUDIO



## Universal Audio Jack

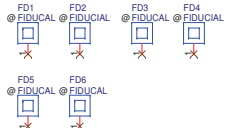
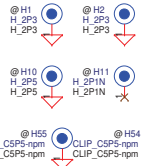
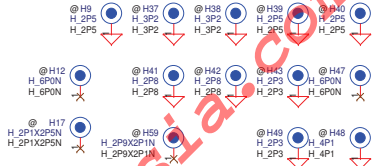
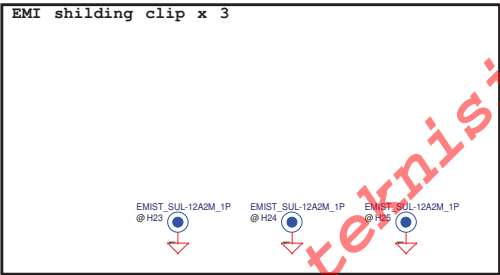
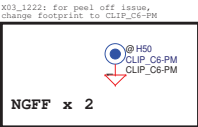
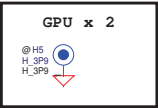
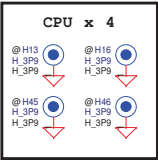


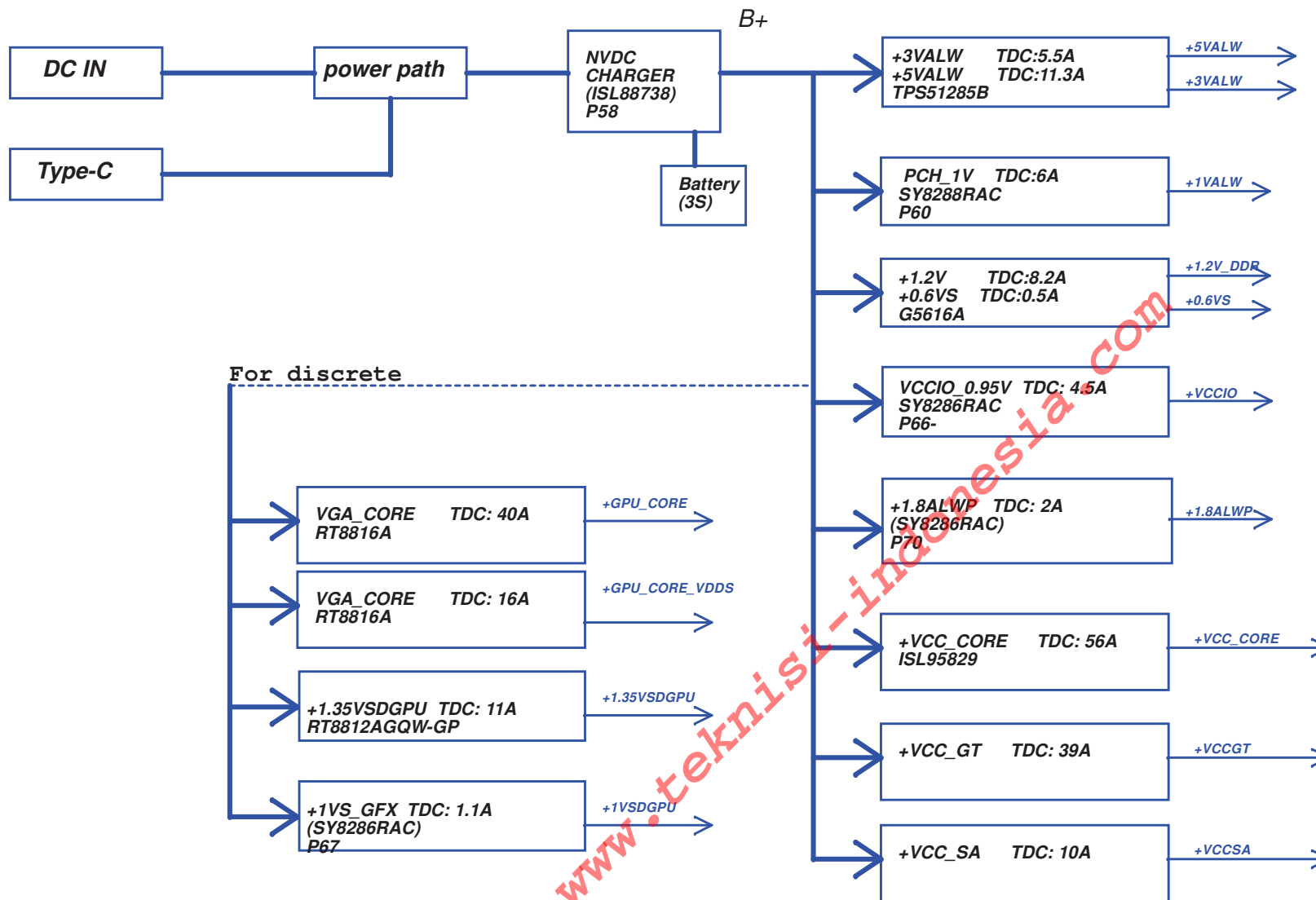
## 1.2V DDR discharger



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				LA-F541P
				Rev 0.1(200)
				Date: Friday, March 23, 2018
				Sheet 53 of 76

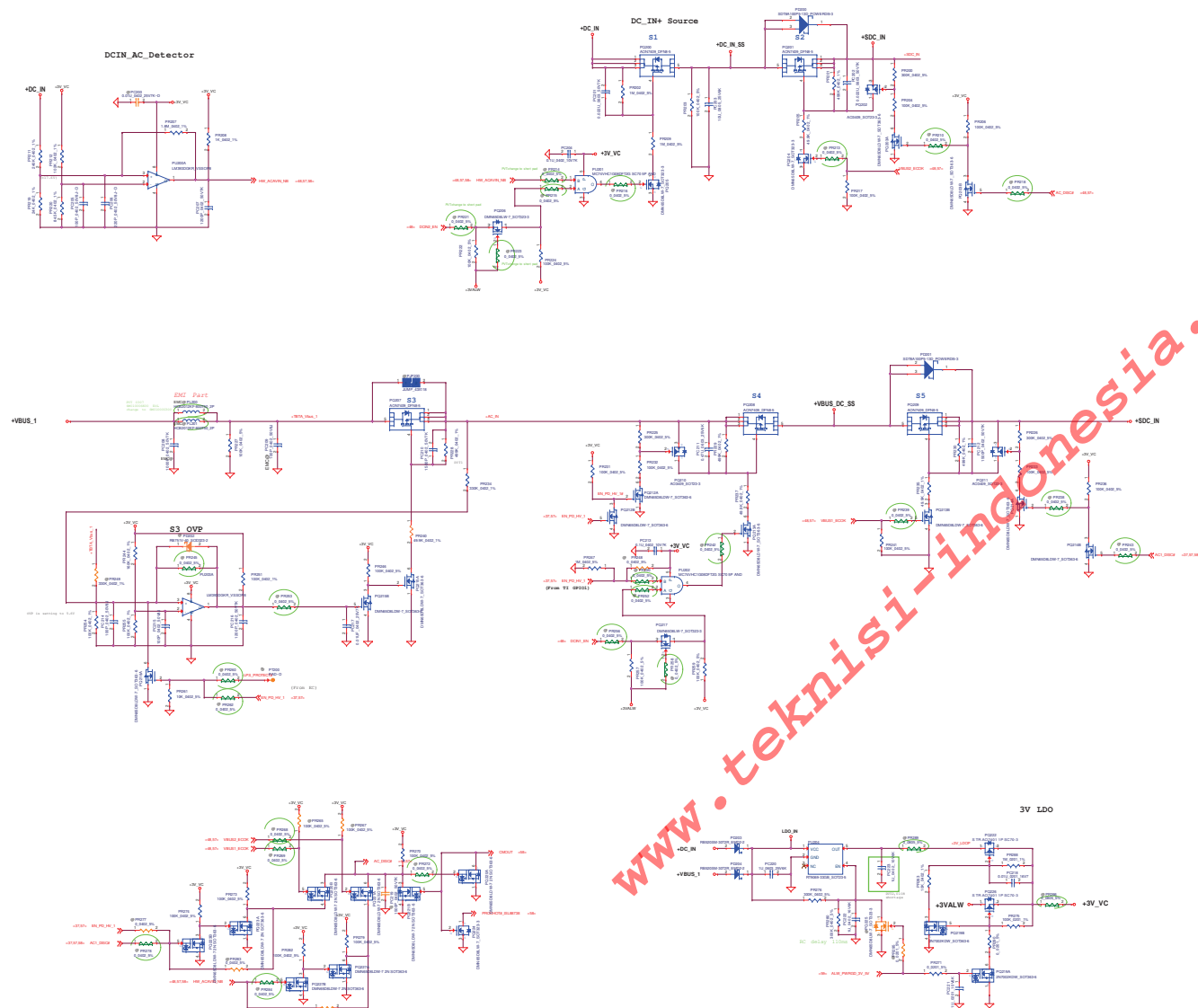
Screw Hole





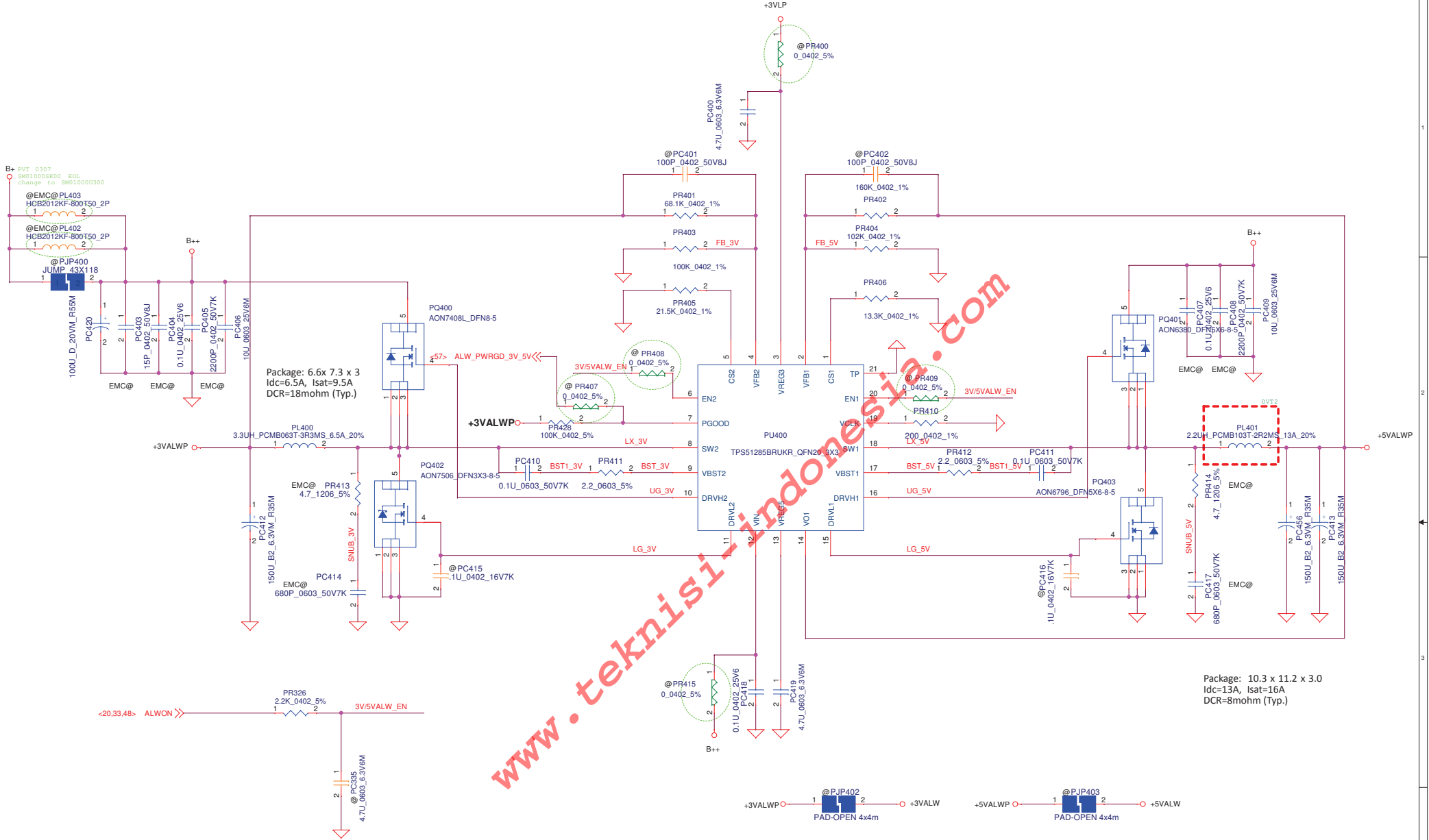
@ : Nopop Component  
 @DIS@ : Nopop Component  
 DIS@: POP for discrete GPU SKU





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3V/5V controller(35.1), Support component(35.2)

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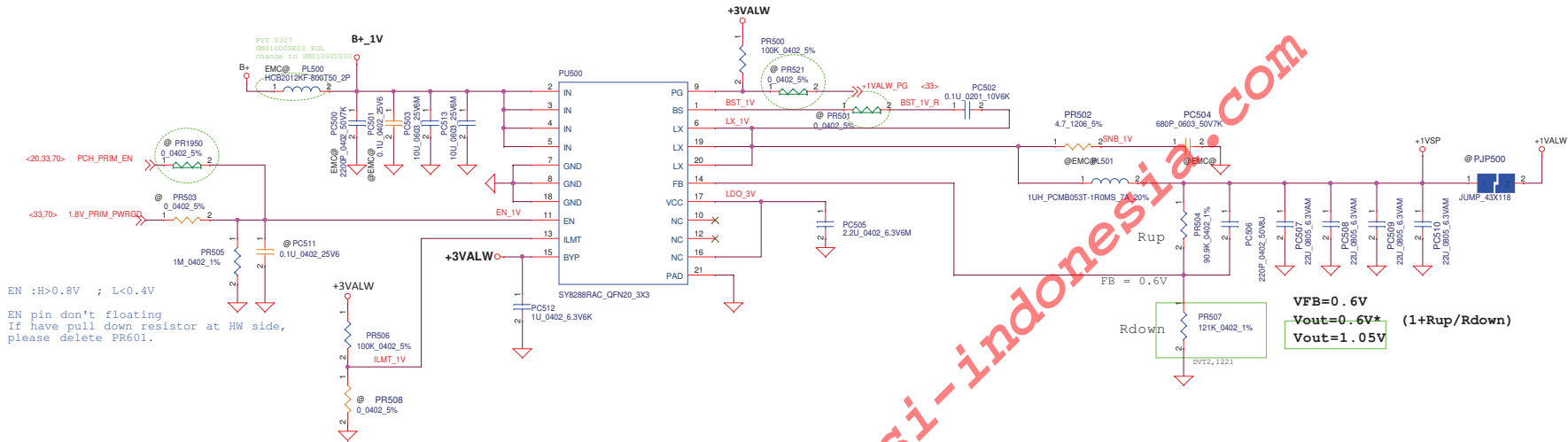


Compal Electronics, Inc.		
Title	P59-PWR 3.3VALWP/5VALWP	
Size	Document Number	Rev
	LA-F541P	0.1(00)
Date:	Friday, March 23, 2018	Sheet 59 of 74

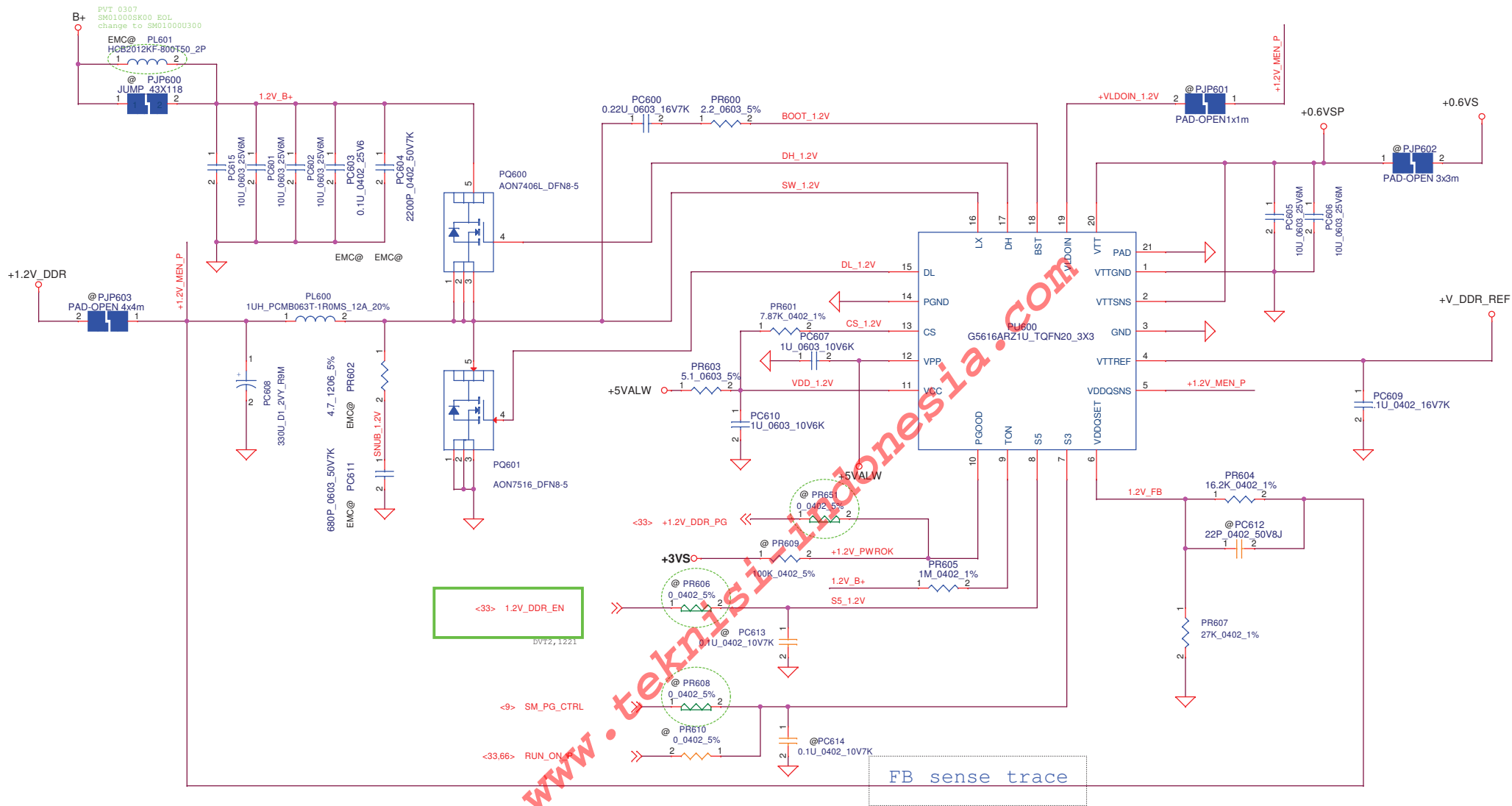
3.3VALWP  
TDC 5.5A  
Peak Current 7.7A  
OCP current 9.35A

5VALWP  
TDC 11.3A  
Peak Current 12.6A  
OCP current 19.2A

+1VSP  
TDC 6A  
Peak Current 8.2A  
OCP current 12A(fix)



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Issued Date	2017/06/21	Deciphered Date	2027/06/21	Title
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				Size Document Number
				LA-F541P
				Rev 0.1(200)
				Date: Friday, March 23, 2018 Sheet 60 of 74



1.2Volt +/- 5%  
TDC 8.2A  
Peak Current 15.4A  
OCP current

0.6Volt +/- 5%  
TDC 0.5A  
Peak Current 0.7A  
OCP Current 0.85A

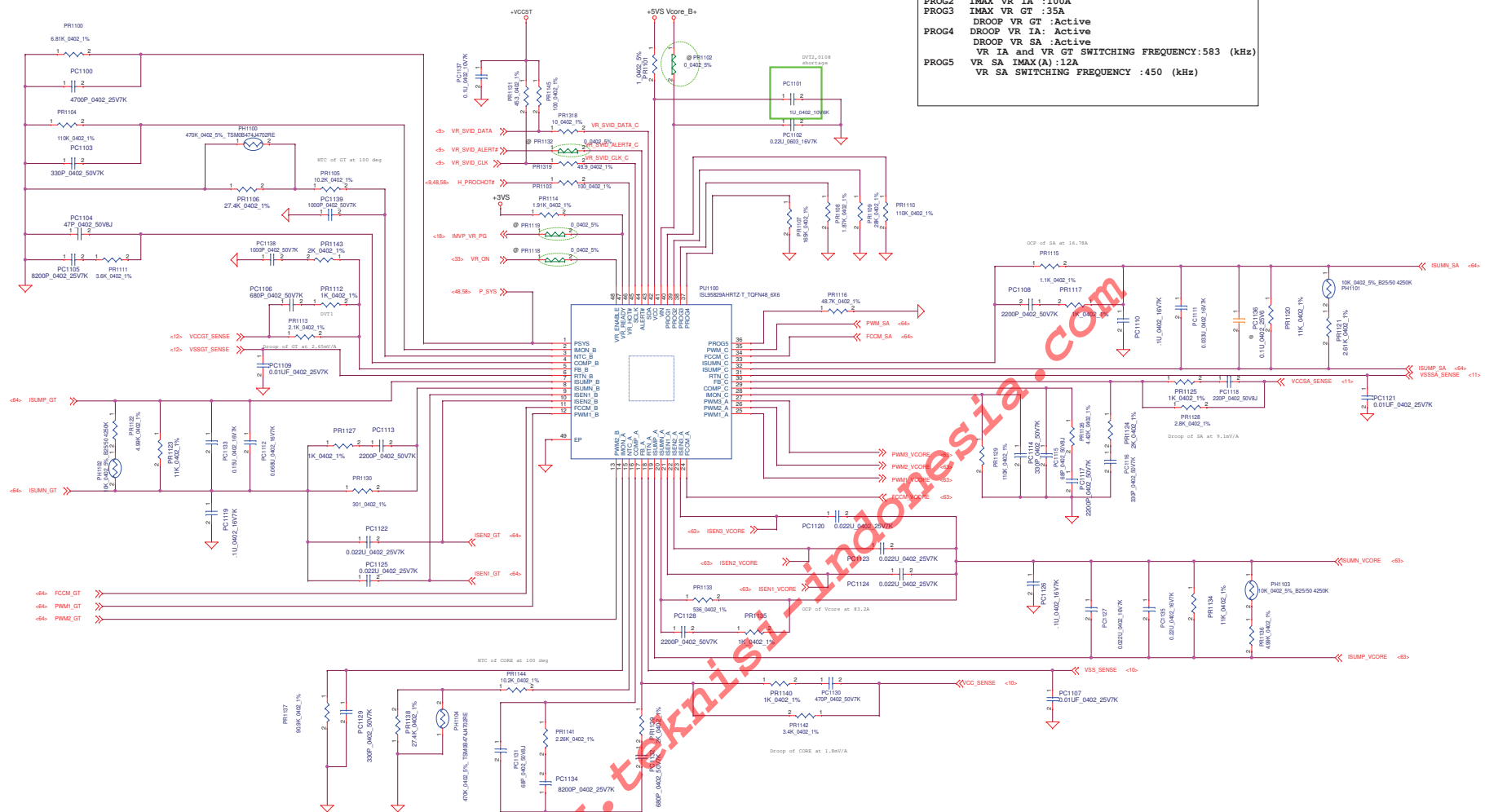
DDR controller(35.3), Support component(35.4)

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<b>Compal Electronics, Inc.</b>			
Title <b>P61-PWR +1.2V MEN/+0.6V DDR</b>			
Size	Document Number		Rev 0.1
	<b>LA-F541P</b>		
Date:	Friday, March 23, 2018		Sheet 61 of 74

PROG sets  
 PROG1 Vboot :0V  
 PROG2 slew rate :30 mV/uS  
 PROG3 IMAX VR IA :100A  
 PROG4 DROOP VR GT :Active  
 DROOP VR IA :Active  
 VR IA and VR GT SWITCHING FREQUENCY:583 (kHz)  
 VR SA IMAX(A):12A  
 VR SA SWITCHING FREQUENCY :450 (kHz)

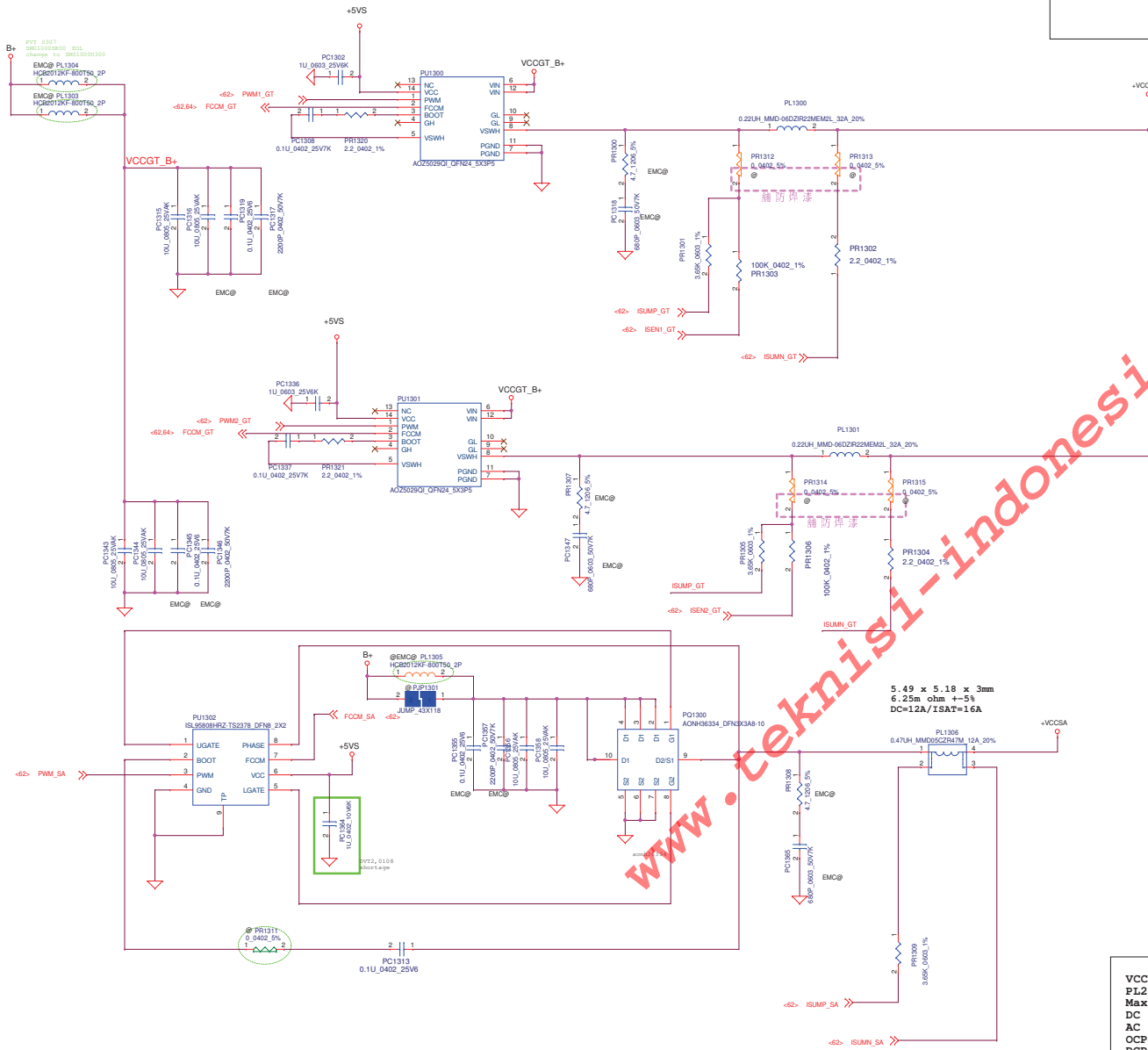


CPU\_Vcore controller(36.1), Drivers(36.2), Support component(36.3)  
 Acoustic Noise B+ Bulk CAP(37.2)

File	PSD-PWR-VCORE_ISL9629
Doc	Document Number
Customer	LA-594-P
Date	Friday, March 23, 2018
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Rev	0.10000



```
VCCGT
PL2 TDC_max (10Sec):25A
Max Current 32A
DC Load line -2.65mV/A
AC Load line -2.65mV/A
OCP Current 48A
DCR 0.98mohm +/-5%
```



```
VCCSA
PL2 TDC_max (10Sec):10A
Max Current 11.1A
DC Load line -9.1mV/A
AC Load line -9.1mV/A
OCP Current 20A
DCR 6.2 ± 5% mOhm
```

CPU\_Vcore controller(36.1), Drivers(36.2), Support component(36.3), GFX output CAP(36.5)

Title			
P64-PWR_VCORE_VGT_VSA			
Size	Document Number		Rev
Customer	LA-F541P		0.1(x00)
Date:	Friday, March 23, 2018	Sheet	64 of 74

+VCC CORE  
470uF\*2  
220uF\*1  
22uF\*40  
1uF\*24

+VCCGT  
470uF\*2  
220uF\*1  
22uF\*40  
1uF\*12

3x 47uF 0805
7x 22uF 0603
10x 10uF 0402
1x 1uF 0201

5x 47uF 0805
11x 22uF 0603
21x 10uF 0402
24x 1uF 0201
24x 0201 (bleeder)

Bulk Decoupling Locations	EXAMPLE
Vcc Power Plane at VR output	3x 220uF
VccGT Power Plane at VR output	3x 220uF
VccGT Power Plane at VR output	3x 47uF 0805
VccSA Power Plane at VR output	3x 47uF 0805

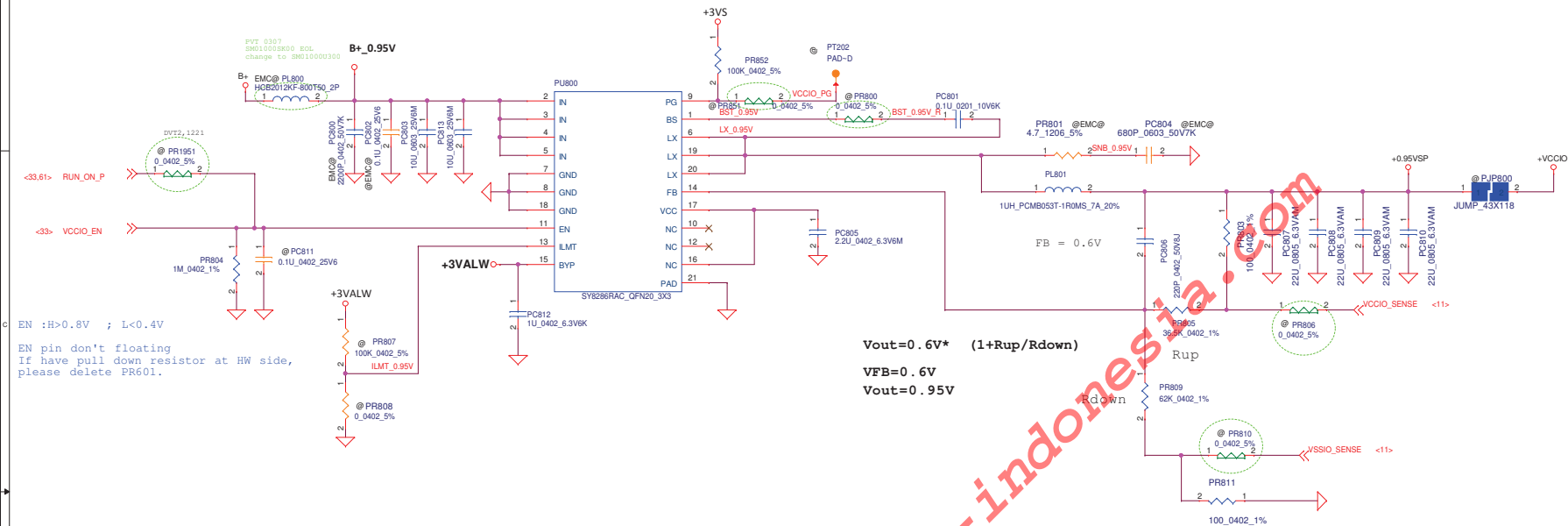
3x 47uF 0805
2x 22uF 0603
7x 10uF 0402

+VCCSA  
22uF\*9

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FORM: P65-PVR-PROCESSOR-DECOUPLING			
Rev: 1.0 (1/00)			
Date: 2017/06/21			
Page: 1 of 1			

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+0.95V	
TDC 4.5A	
Peak Current	6.5A
OCP current	9A (fix)


$$V_{out} = 0.6V \cdot (1 + R_{up}/R_{down})$$
$$V_{FB} = 0.6V$$
$$V_{out} = 0.95V$$
[illegible]

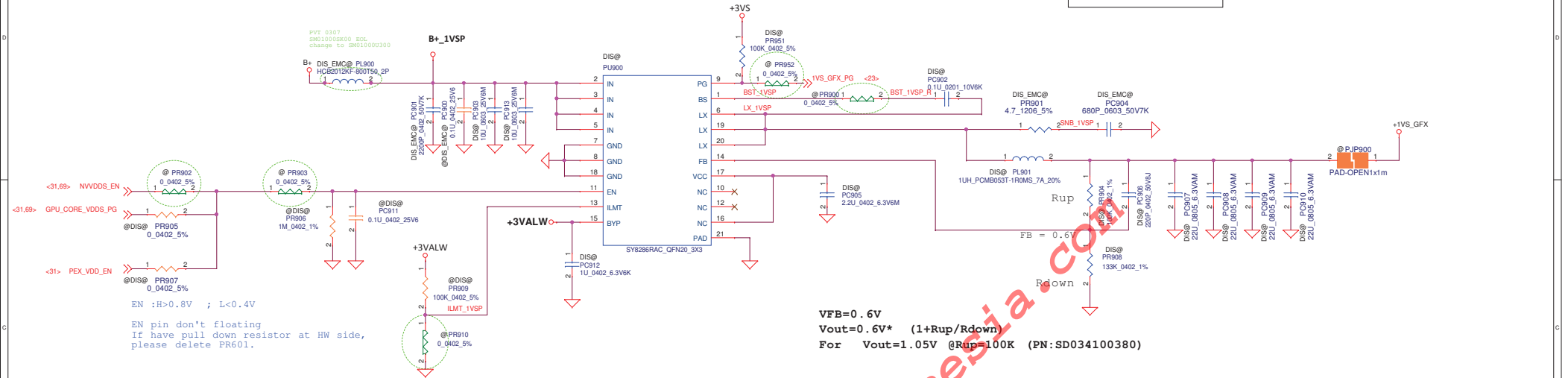
The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

1.05V controller(35.5), Support component(35.6)

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				Date: Friday, March 23, 2018	Sheet	66 of 74

for dGPU SKU  
@DIS@ : Nopop Component  
DIS@: POP for dGPU SKU

+1.0VSP/1.05VSP  
TDC 1.1A  
Peak Current 1.1A  
OCP current 6A(fix)



The current limit is set to 6A, 8A or 12A when this pin  
is pull low, floating or pull high

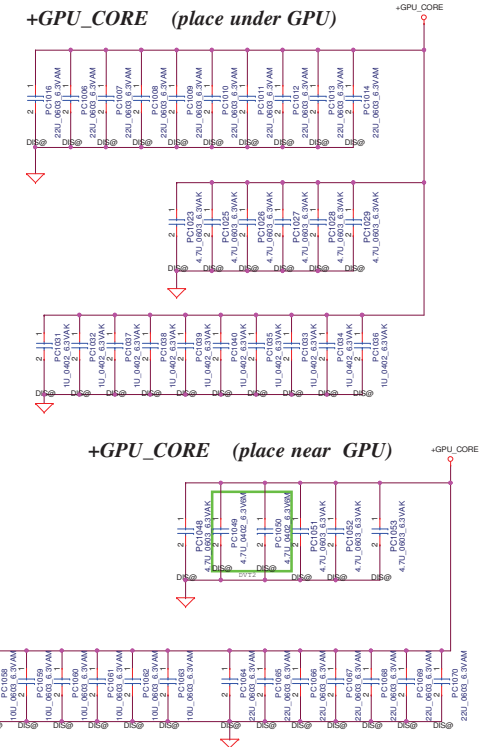
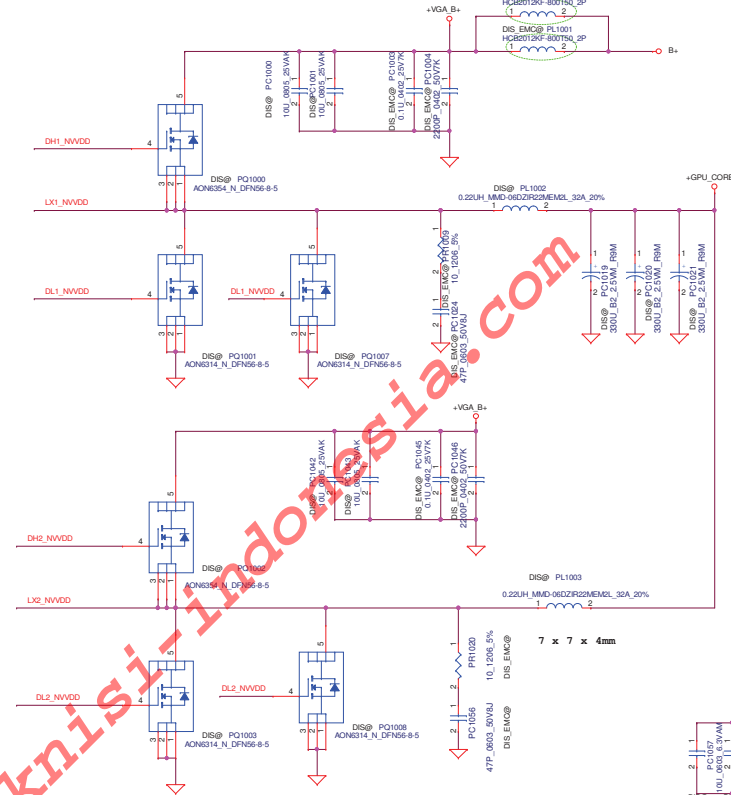
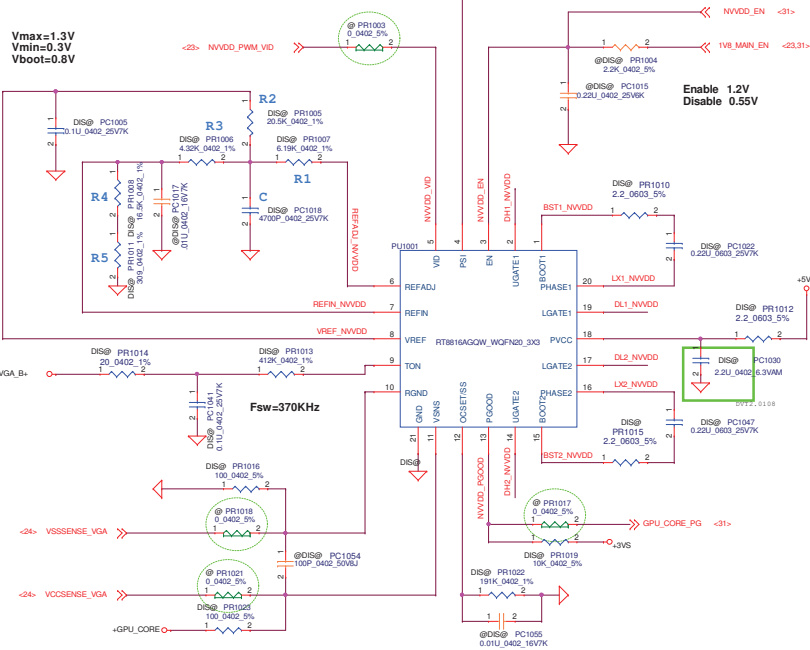
GPU other power\_Regulatorr(43.7), Support component(43.8)

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2017/06/21	Deciphered Date	2027/06/21	Title	P67-PWR +1.05VSDGPU(SY8286RAC)	
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					LA-F541P	0.1(200)
				Date:	Friday, March 23, 2018	Sheet 67 of 74

```
for dGPU SKU
@DIS@ : Nopop Component
DIS@: POP for dGPU SKU
```

2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

```
GPU_CORE (0.95V)
TDC 41A
Peak Current 94A
OCP current 100A
DCR 0.98mohm +/- 5%
```



Under:  
4.7U\_0603\_6.3VAK \*16  
1U\_0402\_6.3VAK \*10


Near:  
10U\_0805\_6.3V6M\*7  
22U\_0805\_6.3V6M \*7  
4.7U\_0805\_6.3V6K \*6  
330u\*3

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VGA\_CORE controller(43.1), Support component(43.2)  
VGA\_CORE Drivers (43.3), GPU Core Output CAP (43.9)

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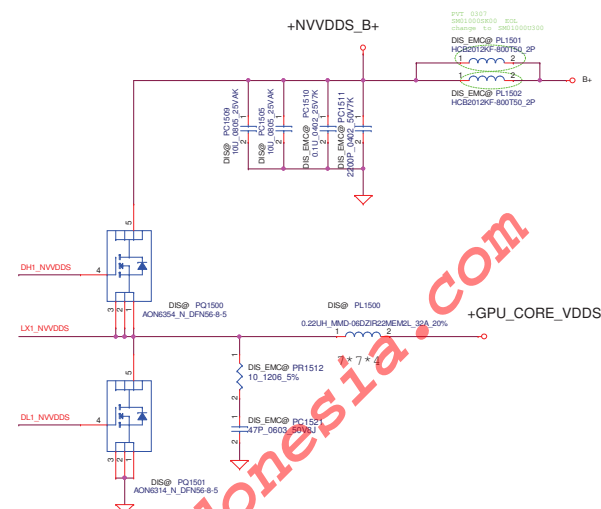
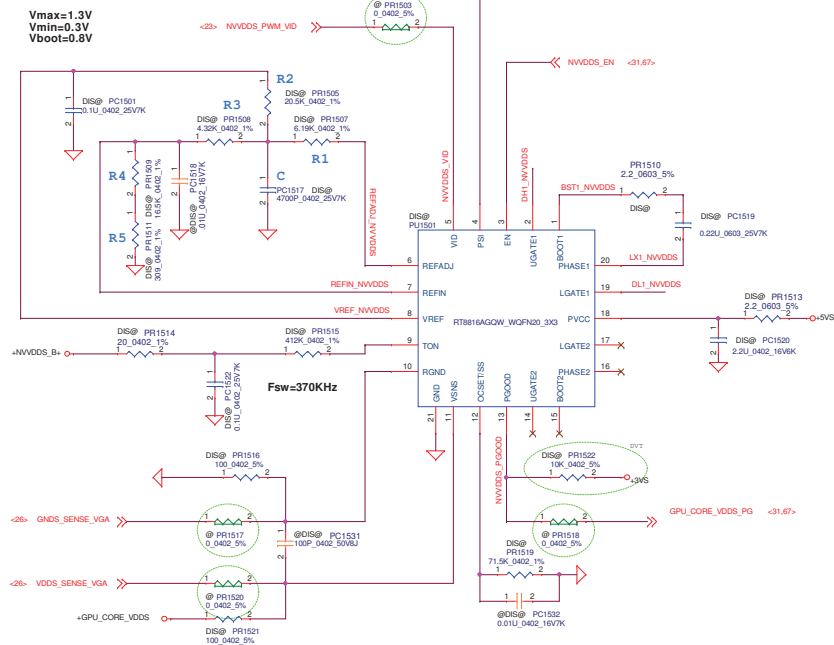
	<b>Compal Electronics, Inc.</b>		
	<b>P68-PWR+GPU CORE</b>		
	<b>LA-F541P</b>		
	Date: Friday, March 23, 2018	Sheet 66 of 74	Rev 0.1(000)

```
for dGPU SKU
@DIS@ : Nopop Component
DIS@: POP for dGPU SKU
```

Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V

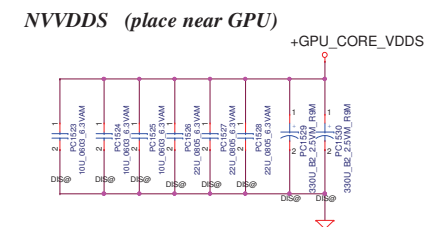
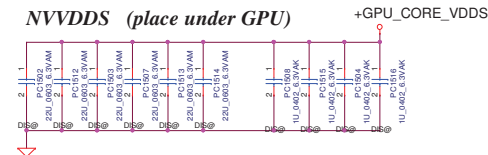
```
+GPU_CORE_VDDS
TDC 12A
Peak Current 16A
OCP current 21A
DCR 0.98mohm +/- 5%
```

		MIN	MAX
H/S	Rds (on)	: 3.7mohm	, 4.5mohm
L/S	Rds (on)	: 1.5mohm	, 1.9mohm



Under:  
4.7U\_0603\_6.3VAK \*6  
1U\_0402\_6.3VAK \*4

Near:  
10U\_0603\_6.3V6M \*3  
22U\_0805\_6.3V6M \*3  
330u\*2

[illegible]

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- VGA\_CORE controller(43.1), Support component(43.2)
- VGA\_CORE Drivers (43.3), GPU Core Output CAP (43.9)

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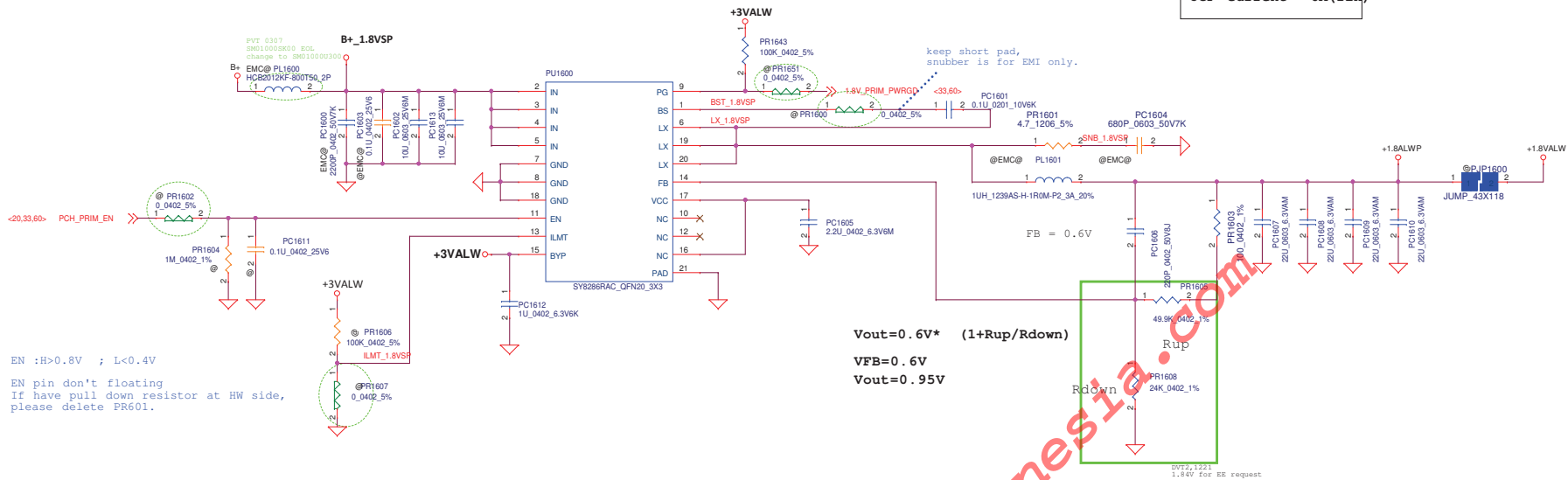
### P69-PWR-+GPU CORE VDDS

LA-F541P

Rev	0.1(200)
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LA-F541P

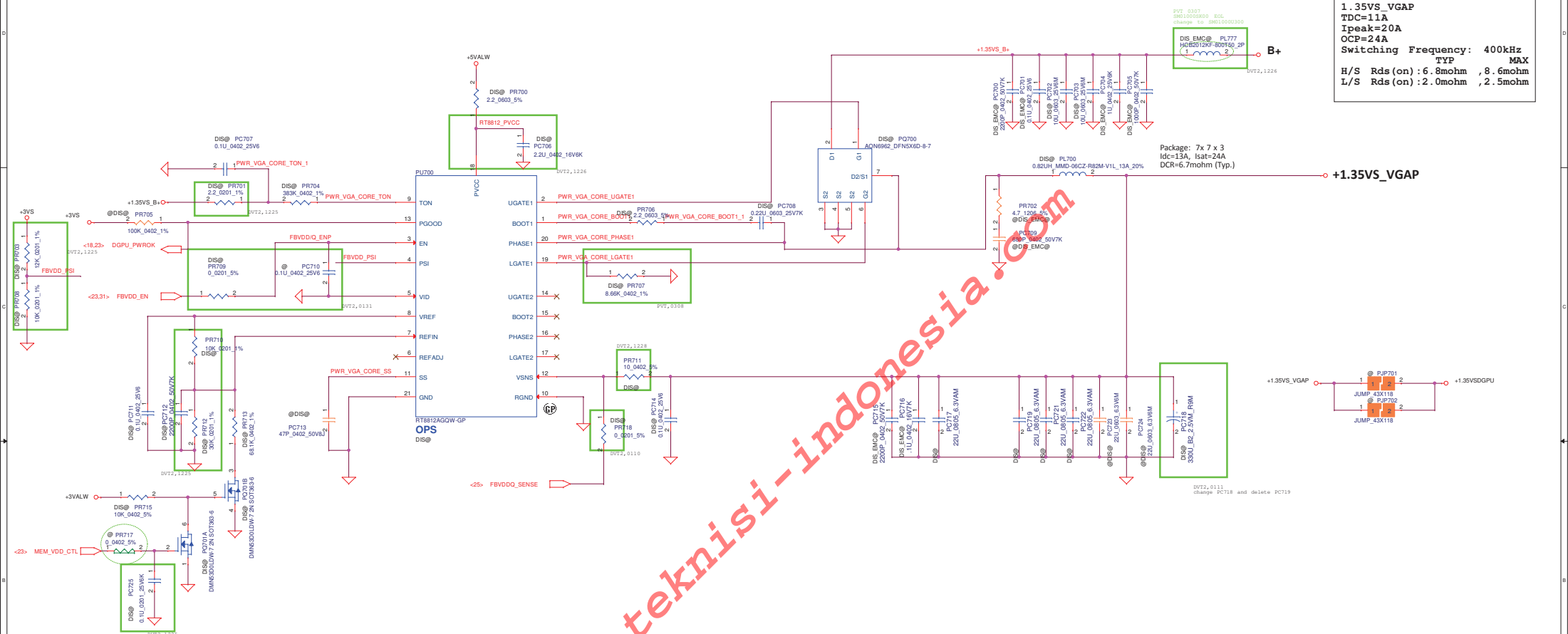
Date: Friday, March 23, 2018 11:02 AM of 74



+1.8VALW  
TDC 2A  
Peak Current 3A  
OCF current 6A(fix)

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Size	C	Document Number		Rev
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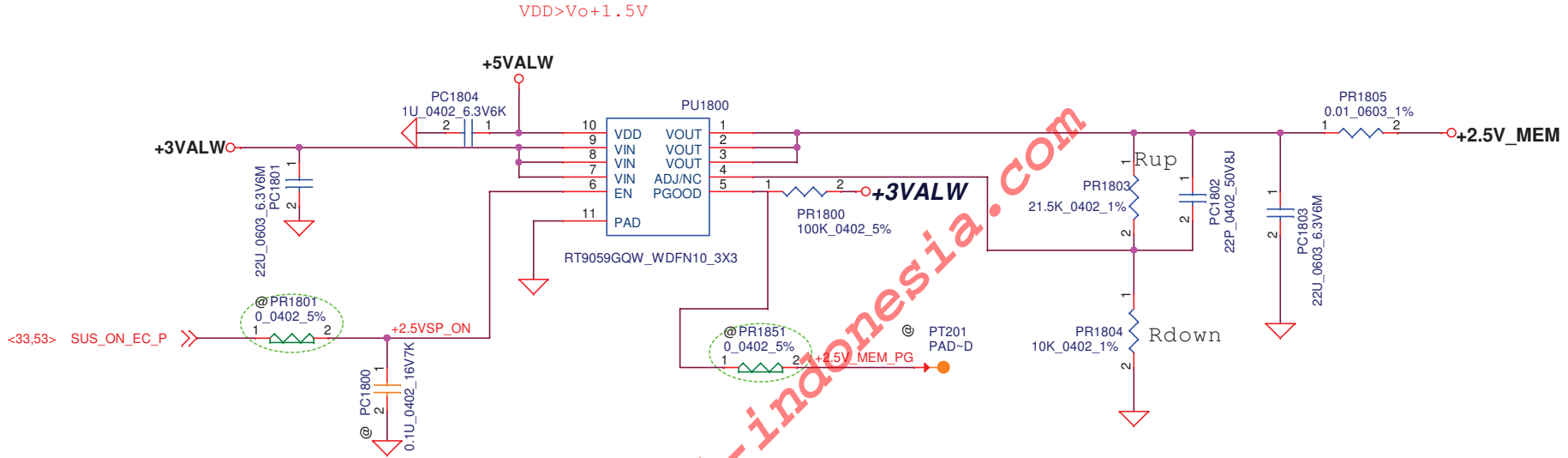
MEM_VDD_CTL	VOUT
L	1.35V
H	1.5V/1.55V



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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title
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2.5V\_MEM controller(35.13), Support component(35.14)

```
+2.5V_MEM
TDC 0.86A
Peak Current 1A
OCP Current 1.46A
```

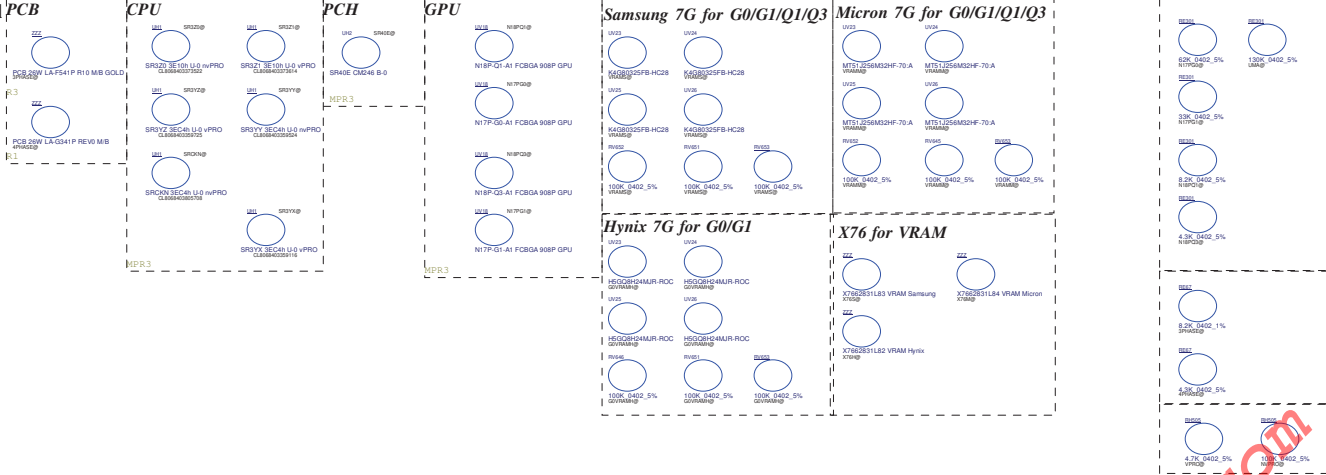


Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
Issued Date	2017/06/21	Deciphered Date	2027/06/21	Title <b>P72-PWR +2.5V MEM(RT9059GSP)</b>		
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					<b>LA-F541P</b>	0.1(X00)
				Date: Friday, March 23, 2018	Sheet 72 of 74	

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
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8				EE			X01
9				EE			X01
10				EE			X01
11				EE			X01
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35				EE			
36				EE			
37				EE			
38				EE			
39				EE			
40				EE			
41				EE			

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Project Code :  
File Name :



RE301	CE3319	CONFIG
240K	4700p	
130K	4700p	UMA
62K	4700p	N17P-G0
33K	4700p	N17P-G1
8.2K	4700p	N18P-Q1
4.3K	4700p	N18P-Q3
2K	4700p	
1K	4700p	

RE67	CE51	REV	PHASE
240K	4700p	X00	EVT
130K	4700p	X01	PRE DVT
62K	4700p	X02	DVT1
33K	4700p	X03	DVT2
8.2K	4700p	A00	PVT
4.3K	4700p	X00 4P	I9 EVT
2K	4700p	X01 4P	I9 DVT
1K	4700p	A00 4P	I9 PVT

T15 CONFIDENTIALITY	
HIGH(4.7K)	vPRO
LOW(DEFAULT)(1.00K)	non-vPRO
WCS 238 internal pull-down	

DRAM Option

DRAM Config Option

DRAM SDP / DDP Option

R\_COMP

X76

SDP	MEM_CONFIG0	MEM_CONFIG1	MEM_CONFIG2	MEM_CONFIG3	MEM_CONFIG4	R_COMP	X76
MICRON 8G/2400							X7674531L07
SDP							X7674531L09
SDP							X7674531L08
SDP							X7674531L10
DDP							X7674531L15
DDP							X7674531L11

